Analysis of trap effect on reliability using the charge pumping technology in La-incorporated high-k dielectrics

Hyuk-Min Kwon, Won-Ho Choi, In-Shik Han, Sang-Uk Park, Byoung-Seok Park, Ying-Ying Zhang, Chang-Yong Kang, Byoung-Hun Lee, Raj Jammy, Hi-Deok Lee

Department of Electronics Engineering, Chungnam National University, Yusong-Gu, Daejeon 305-764, South Korea
International SEMATECH, 2706 Montopolis Drive, Austin, Texas 78741, USA
Department of Materials Science and Engineering, Gwangju Institute of Science and Technology (GIST), Buk-Gu, Gwangju 500-712, South Korea

Abstract

In this paper, reliability characteristics of nMOSFETs with La-incorporated HfSiON and HfON and metal gate have been studied. HfLaSiON shows greater device degradation by hot carrier (HC) stress than by positive bias temperature (PBT) stress, while HfLaON exhibits similar degradation during HC stress and PBT stress. To evaluate the contribution of bulk trap during PBT stress, a novel charge pumping (CP) technique is applied to extract the distribution of bulk trap (Nbt) before and after PBT stress. To evaluate permanent damage during HC stress, an appropriate selection of frequency range in CP method is considered. The initial interface trap density of HfLaSiON and HfLaON is similar, while the near-interface trap (NIT) density of HfLaSiON after HC stress is equal or greater than that of HfLaON.

1. Introduction

The integration of metal gate (MG)/high-k (HK) into CMOS technology still has several issues such as a high threshold voltage (VT), which is believed to be due to Fermi-level-pinning effect between the MG and the HK [1,2], and MG/HK reaction or oxygen vacancy at MG/HK dielectric interface. To overcome these problems, mixing of a HK dielectric with a rare-earth metal has been proposed as a promising approach for further engineering of the dielectric properties in materials and for improving their electrical performance and reliability [3,4]. However, reliability is still a critical factor due to a high trap density of structural defects in HK (metal oxide) [5]. The traps generated by stress induced defect in HK gate dielectrics and interface region have been extracted to find out the critical factor of reliability mechanism [6,7]. The efficient extraction of stress induced trap generation in HK gate dielectrics can be achieved by charge pumping method with various frequencies and rise/fall time [8–10]. Recently, lanthanum (La)-incorporation into HfSiO or HfO2 has been reported for improvement of the electrical performance, easy VT control, and reduction of gate leakage current by the formation of dipole moment due to the diffusion of electropositive La to the HK/SiO2 interface [11]. However, there was a little report on comparative and comprehensive analysis of reliability properties which can be affected by the traps generated at the interfacial SiO2 layer (IL) and HK gate dielectrics.

In this paper, a comparative analysis of reliability of nano-scale MOSFETs with La-incorporated HfSiO and HfO2 is performed through the analysis of the interface and bulk effects on reliability. Charge pumping method is used to evaluate the trap generation at the IL and HK dielectric during HC stress and PBT stress.

2. Experimental details

Conventional gate-first standard CMOS process is used to fabricate MOSFETs on p-type silicon substrate. After formation of shallow trench isolation, HfSiO or HfO2 film was deposited on ultrathin SiO2 by atomic layer deposition (ALD), followed by a post-deposition treatment with NH3 ambient. Then, ultrathin (0.5 nm) lanthanum oxide (La2O3) is deposited on the HfSiO or HfO2 by a molecular beam deposition (MBD). TaN (10 nm) MG was deposited by reactive sputtering on the dielectric stack and capped with poly-Si. After source/drain (S/D) implantation, a 1070 °C spike annealing is applied for source/drain activation. Both the La-incorporated...
HfSiON and HfO₂ dielectrics have the same final physical thicknesses (tPHY ≈ 2.5 nm).

3. Results and discussion

Fig. 1 shows trapping and de-trapping characteristics of MOSFETs with HfLaSiON and HfLaON under positive bias temperature (PBT) stress (VG − VTH = 1.8 V, 125 °C) and hot carrier (HC) stress (VG = VD = VTH + 1.8 V, 25 °C). Such VTH shift behavior by PBT stress is consistent with the phenomenon of injected electron trapping/de-trapping at the pre-existing bulk trap [12]. The small, unrecovered VTH shift of HfLaSiON (16.132 mV) and HfLaON (75.347 mV) suggests that traps can be generated within the interface layer (IL) and high-k (HK) gate dielectrics. As reported in [13], more degradation under HC stress than PBT stress in short channel devices is due to the combined effects of cold carrier and hot carrier as shown in Fig 2. However, it is notable that HfLaON exhibits more degradation than HfLaSiON while the slope of VTH shift for HfLaSiON by HC stress is 1.5 times greater than that of HfLaON, which implies higher generation rate by HC stress as shown in Fig 3. Therefore, La doping into HfO₂ and HfSiO can modify the interface characteristics due to the dipole moment at the HK/SiO₂ interface [11].

Fig. 4 shows a degradation slope of $G_{m,\text{max}}$ during PBT and HC stresses and during recovery with $V_G = −1\,\text{V}$ after 2000 s and 6000 s. The degradation slope of $G_{m,\text{max}}$ of HfLaSiON is similar to that of HfLaON for PBT stress, while it is greater than that of HfLaON for HC stress as shown in Fig 4. The higher $G_{m,\text{max}}$ degradation means greater HC effect and no significant recovery, which can be affected by the permanent damage in IL by HC stress [14].

To ensure an accurate assessment of trap generation, further study of the charge trapping and de-trapping is required to extract trap effect using charge pumping measurement [15–16]. Fig. 5 presents the frequency dependent trap density extracted using the charge pumping method. The initial interface trap density of HfLaSiON and HfLaON at high frequency region is similar, while there is greater initial bulk trap density of HfLaON than HfLaSiON at low frequency region. The bulk trap density of two devices at low frequency increases greatly after stress, while only small increase is detected at higher frequencies like in [10]. The difference of trap density between PBT stress and HC stress for HfLaSiON is greater than that of HfLaON as marked by circles in Fig 5, which implies higher generation rate of interface traps due to permanent damage by HC stress for HfLaSiON. Hence, analysis of trap effect by stress is necessary to separate interface region and bulk region using CP technology, which can separate charge trapping and permanent damage range as marked by circles in Fig 5. F–N fitting of gate currents shows higher barrier height of HfLaON than HfLaSiON as shown in Fig 6.
To estimate the location of traps with respect to the Si-substrate and energies of traps in HK gate dielectrics [17], capture cross section is extracted using different rise/fall time (t_r/t_f) as shown in Fig 7. Capture cross section is a key parameter for the carrier tunneling in HK gate dielectrics and necessary to obtain the near-interface trap (NIT) distribution with energy and spatial dependence [17].

Capture cross section and the energy distribution of interface trap density (D_{it}) of HfLaON are greater than HfLaSiON, which can provide the analysis of reliability characteristics as shown in Fig 7.

Fig. 8 shows the magnitude of charge pumped per cycle (Q_{cp}) as a function of rise/fall time, (a) HfLaSiON and (b) HfLaON. The capture cross section and D_{it} of HfLaON are higher than those of HfLaSiON.

To analyze the interface trap density after HC stress, profile of near-interface traps (NIT) is plotted as functions of energy and tunneling depth using the charge fall time of charge pumping technology as a function of the distance are shown in Fig. 9, which is extracted from the Q_{cp} versus frequency curves before and after PBT stress as shown in Fig. 8. The increase of bulk trap at low frequency after PBT stress indicates the effect of generated traps, thus, high charge trapping of HfLaON can be attributed to high pre-existing bulk trap density.

To analyze the interface trap density after HC stress, profile of near-interface traps (NIT) is plotted as functions of energy and tunneling depth using the charge fall time of charge pumping technology.
where \( N_{\text{IT}} \) (depth \( d \)) is the energy distribution of near-interface trap density of \( n\text{MOSFET} \) for Fig. 10.

Volume densities of bulk traps (\( N_{\text{bt}} \)) in gate dielectric as a function of the distance from Si surface with and without PBT stress. Depth profile of \( N_{\text{bt}} \) for three different CP frequencies. Near-interface traps (\( N_{\text{IT}} \)) of \( \text{HfLaSiON} \) is equal or greater than that of \( \text{HfLaON} \) at the same energy level after HC stress.

4. Conclusions

A comparative study of \( \text{HfLaSiON} \) and \( \text{HfLaON} \) through the analysis of the effect of interface and bulk traps on reliability is performed. Charge pumping method is used to show that the initial interface trap density of \( \text{HfLaSiON} \) and \( \text{HfLaON} \) at high frequency region is similar, while there is greater bulk trap density of \( \text{HfLaON} \) than \( \text{HfLaSiON} \) at low frequency region. It is also shown that bulk trap density of \( \text{HfLaON} \) becomes greater than that of \( \text{HfLaSiON} \) after PBT stress. The near-interface trap density of \( \text{HfLaSiON} \) is equal or greater than that of \( \text{HfLaON} \) at the same energy level after HC stress.

Acknowledgements

This research was partly supported by the Ministry of Knowledge Economy (MKE) and Korea Industrial Technology Foundation (KOTEF) through the Human Resource Training Project for Strategic Technology. This work is also supported in part by the IT R&D program of MKE/KEIT (10034838, Development of Oxide Trench Etcher beyond 25 nm).

References


Fig. 9. Volume densities of bulk traps (\( N_{\text{bt}} \)) in gate dielectric as a function of the distance from Si surface with and without PBT stress. Depth profile of \( N_{\text{bt}} \) for \( \text{HfLaON} \) before and after PBT stress is greater than that of \( \text{HfLaSiON} \).

Fig. 10. Energy distribution of the near-interface trap density (\( N_{\text{IT}} \)) of \( n\text{MOSFET} \) for three different CP frequencies. Near-interface traps (\( N_{\text{IT}} \)) of \( \text{HfLaSiON} \) is equal or greater than that of \( \text{HfLaON} \).