Hot carrier stress study in Hf-silicate NMOS transistors

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Abstract

Hot carrier stress (HCS) effects in NMOSFETs with the HfSiO gate dielectric and poly-Si gate electrode are investigated. Both cold carrier and hot carrier contribute to the reversible V_{th} shift. In the case of the poly gate electrode, the stress bias dependant positive charge, attributed to the hole generation/trapping process, may complicate evaluation of the CVS and HCS. Cold carrier induced hole generation in poly-Si gate devices at high temperature is not desirable for high-k stack. TiN metal gates show superior stress stability.

Introduction

Since electrons can be trapped and de-trapped in the high-k dielectrics with a minimal residual damage to its atomic structure [1-3], the reversible electron trapping, which is not observed in the case of SiO_2 dielectrics, can significantly affect the transistor parameters and complicate the evaluation of the properties of high-k gate stacks, in particular, their response to the hot carrier stress. Both hot carriers near the drain region of the channel and cold carriers (channel electrons) can be injected and trapped in the high-k layer during the hot carrier stress [4,5]. While hot carrier stress is known to generate permanent damages in SiO_2 dielectric, the degradation of certain high-k transistor parameters such as threshold voltage, due to the cold carriers trapping (during CVS) was shown to be reversible [6]. It is, therefore, very important to separate hot carrier-related degradation effects from the cold carrier accumulation in the high-k dielectric. In this paper, we investigate the detail characteristics of V_{th} shift during constant voltage stress (CVS) and hot carrier stress (HCS) to find a way to differentiate the contribution of cold carrier trapping and hot carrier injection using de-trapping bias.

Device fabrication and hot carrier stress

The NMOS transistors were fabricated using 4.5nm Hf-silicate (20%) gate dielectric and poly-Si gate electrode (EOT=19Å). Since the worst-case degradation of the high-k devices under the hot carrier stress has been reported to occur at the $V_g=V_d$ condition [4-5], the 0.15μm NMOS devices were subjected to the hot carrier stress and constant gate voltage stress under the following conditions: $V_g=V_d=2\sim2.4V$ and $V_g=2\sim2.4V$, $V_d=0V$ respectively. The stress was interrupted every one order of the stress duration to measure the drain current, I_d, in a linear regime and the magnitude of the V_{th} shift was monitored for 1,000 seconds to track the charge trapping behavior. After each stress and sensing cycle of 1,000 seconds, the stress bias was removed and negative gate voltages of different values and durations were applied to examine the electron de-trapping characteristics.

Results and discussion

For 0.15um channel devices, the I_{sub} current in HfSiO devices does not show significant decrease at higher V_g values, unlike SiO_2 transistors (Fig 1).

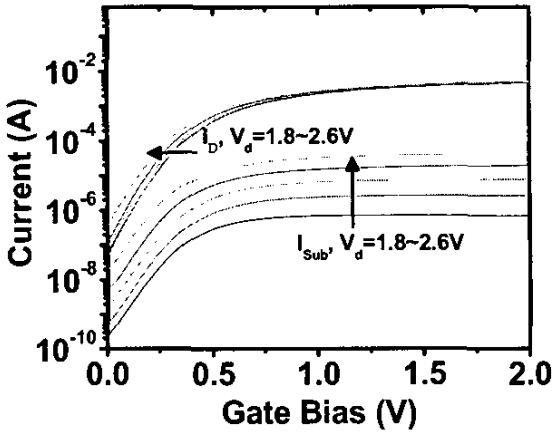

Fig.1 Dependence of I_d-V_g and I_{sub}-V_g curves on drain bias V_d=1.8~2.6V in HfSiO/poly gate stack devices.

This result, which was explained by the localized transient charging model [5], suggests the $V_g=V_d$ condition for the HCS.

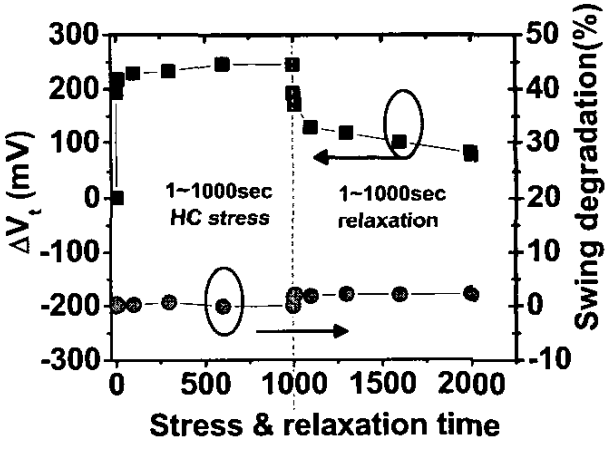

Fig. 2 Threshold voltage shift and subthreshold swing degradation (%) during HC stress ($V_g=V_d=$ 2.2V) and relaxation ($V_g=V_d=0$) in HfSiO/poly-Si devices.

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During the HCS, threshold voltage shift tends to saturate, and significant portion of this shift can be recovered during the relaxation step (V_g=V_d=0) (Fig 2). Negligible subthreshold swing degradation indicates that the electron trapping in the bulk of the dielectric dominates the observed V_{th} shift during HCS. Since cold and hot carrier can contribute to the total V_{th} shift in Fig.3, various characterization methods were used to separate contributions from the cold and hot carriers.

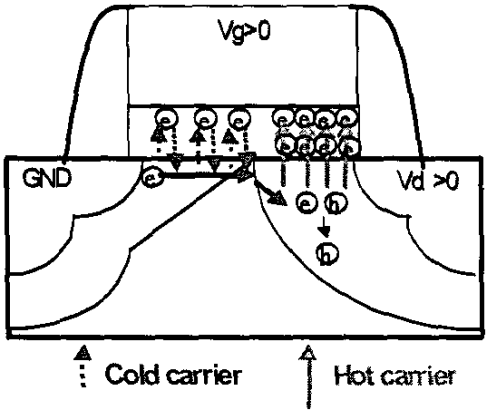

Fig.3 Schematic of the cold and hot carriers injection processes during the HC stress.

First, HC stress was performed repeatedly on the same device followed by a short negative bias stress (for the electron de-trapping) after each HCS cycle. V_{th} shift during the five cycles of HCS and de-trapping (V_g=-1V/10sec) is approximately identical (Fig 4), indicating that electrons were trapping in pre-existing defects rather than generating new traps.

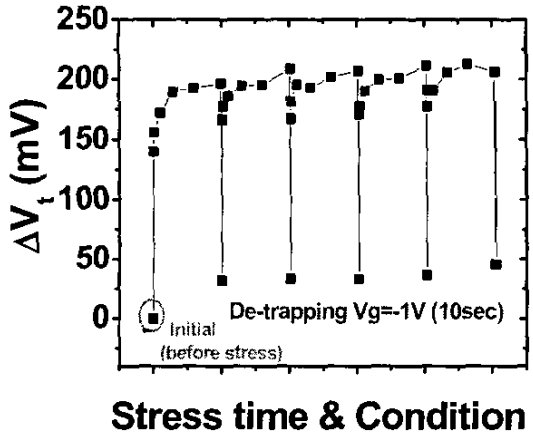

Fig. 4 Threshold voltage shift during five cycles of HC stress (V_g, V_d=2V/ 1000sec) followed by the de-trapping step.

The optimum de-trapping bias condition, V_g=-1V, which would not generate additional positive charges in the dielectric, was obtained by performing stress on fresh devices with different negative biases (Fig 5).

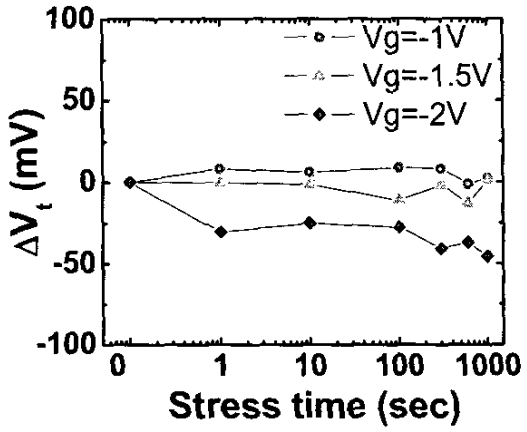

Fig. 5 Threshold voltage shift during the negative bias stress.

Using the above de-trapping conditions, the differences between CVS and HCS are studied. At the same gate bias, HCS appears to induce larger positive V_{th} shift than CVS, before and after de-trapping bias applied (Fig. 6), pointing to an increased contribution from the hot electrons.

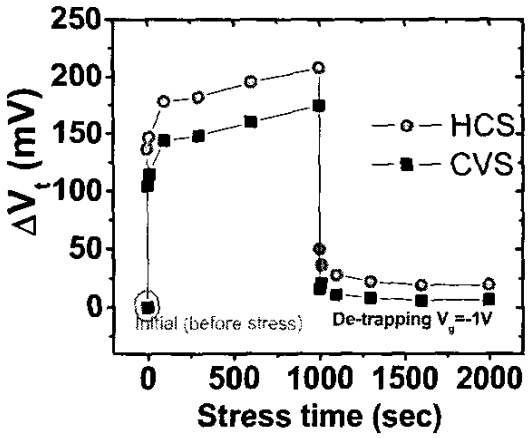

Fig. 6 Threshold voltage change during HC stress (V_g =V_d=2V) and CVS (V_g=2V, V_d=0) followed by the de-trapping step (V_g=-1V).

At the three different stress conditions, similar trends of HCS induced positive V_{th} shift (Fig. 7) appears to induce larger positive V_{th} shift than CVS (Fig. 8). During the negative gate

bias stress (-1V/1000sec, for the electron de-trapping) followed HCS or CVS, additional negative V_{th} shift (V_{th} values were below the initial pre-stress V_{th}) was observed when HCS and CVS were performed with higher positive voltages (Figs. 7, 8). Since –1V stress does not generate positive charges in the dielectric (Fig. 5), the observed negative V_{th} shift was attributed to the holes generated at the poly-Si gate electrode by injected electron impact; the hole may then diffuse towards the Si substrate interface producing negative V_{th} shift. After electron de-trapping by applying negative gate bias, larger negative V_{th} shift reflects greater hole generation/diffusion efficiency of CVS with respect to HCS.

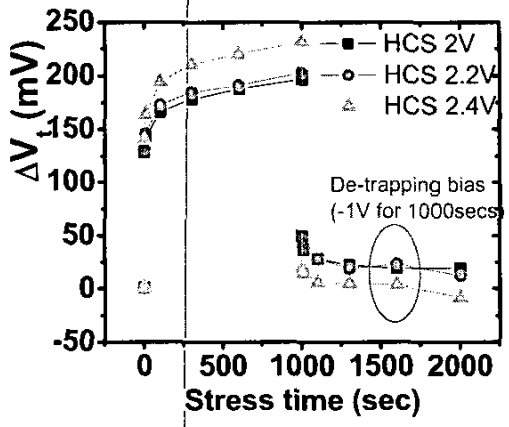

Fig. 7 Threshold voltage shift time dependence during HCS (1000secs) followed by the negative bias stress.

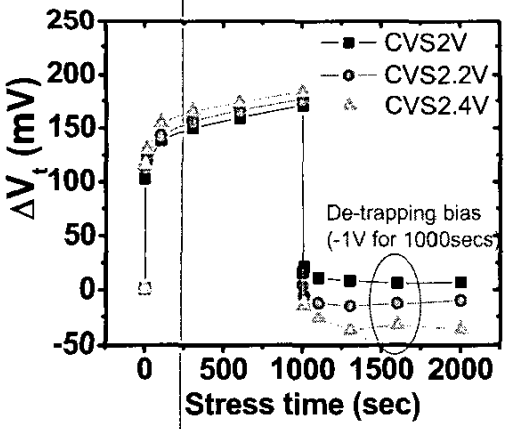

Fig. 8 Threshold voltage shift time dependence during CVS (1000secs) followed by the negative bias stress.

Indeed, the difference between CVS and HCS is amplified at higher temperatures. At 150°C, the V_{th} shifts in the CVS case showed much stronger gm degradation than in HCS (Fig 9).

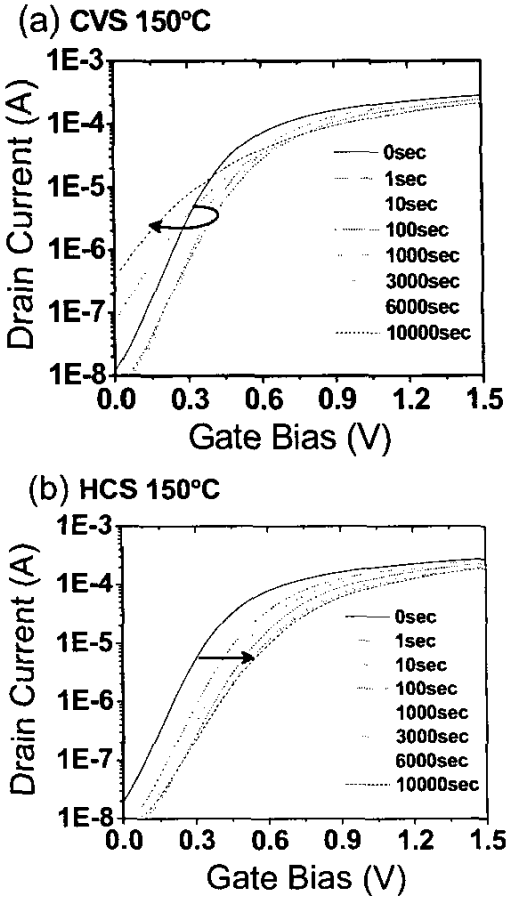

Fig. 9 Changes of the Id-Vg curve with stress time in HCS (V_g=V_d=2.4V) and CVS (V_g=2.4V) at 150°C

This is consistent with the more effective hole diffusion at elevated temperatures: the holes trapped at the dielectric/sub-oxide interface can be responsible for the observed subthreshold swing degradation and additional negative V_{th} shift [7,8]. The issue is why HCS shows significantly smaller swing degradation than CVS. One possible explanation is less electron injection and, subsequently, hole generation due to de-biasing of the drain portion of the gate when the drain bias is applied, as occurred during HC stress. Subthreshold swing degradation is decreased with increasing drain bias at high temperature (150°C), supporting high electron injection generating electron-hole pair and leading swing degradation(Fig 10). If this explanation is correct, no swing degradation during a high temperature CVS or HCS should be expected in the case of a metal gate electrode, which cannot produce electron-hole pairs. Indeed, no swing degradation was observed in the CVS of the transistors fabricated with the same HfSiO dielectric but TiN gate electrode (Fig 11).

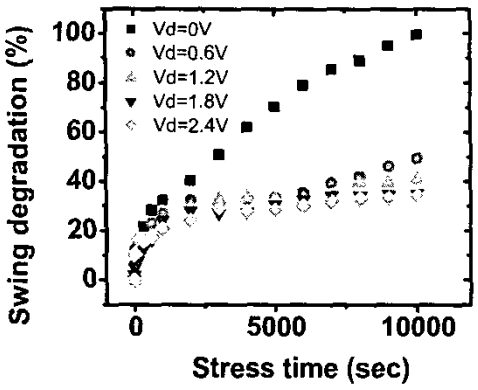

Fig. 10 Time dependence of the threshold voltage swing degradation at different drain voltages during HCS at 150°C (V_g=2.4V)

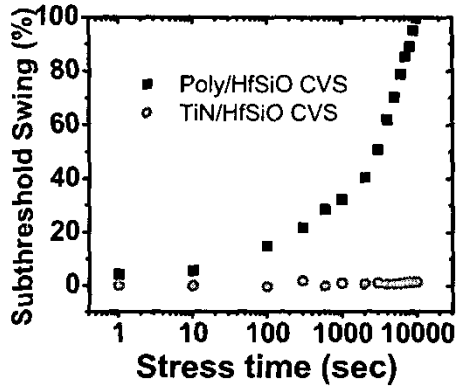

Fig. 11 Swing degradation during the constant voltage stress at 150°C in Poly vs TiN gate electrode transistors

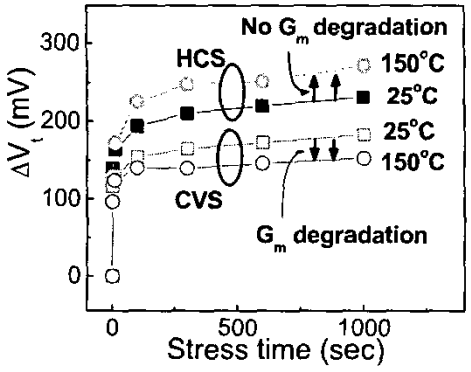

Fig. 12 Swing degradation during the constant voltage stress at 150°C in Poly vs TiN gate electrode transistors

In the case of CVS with poly-si gate electrode, threshold voltage shift at high temperature affected by cold carrier induced hole generation is less than room temperature due to swing and gm degradation. On the other hand, HCS induced threshold voltage shift is increased at high temperature due to less swing and gm degradation (Fig 12). In a summary illustration, non-uniform hot carrier stress induced charge movements in high-k device with poly gate electrode are shown (Fig. 13). This additional transistor parameters instability caused by the electron induced hole generation/diffusion complicates implementation of the high-k gate stacks with the poly-Si gate electrode.

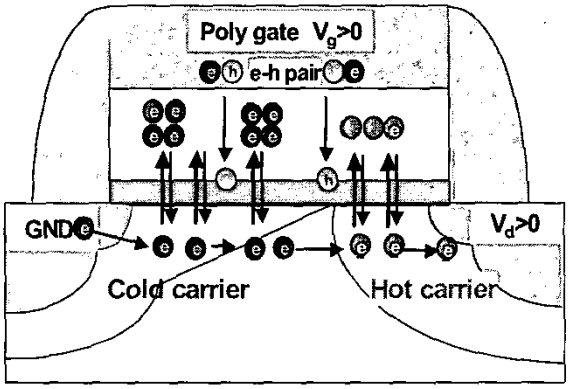

Fig. 13 Non-uniform hot carrier stress induced charge movements in high-k device with poly gate electrode.

Conclusion

Hot carrier stress effects in NMOSFETs with the HfSiO gate dielectric and poly-Si gate electrode were investigated. It was found that both cold carriers and hot carriers contribute to the reversible V_{th} shift. In the case of the poly gate electrode, HCS induce more reversible electron trapping than CVS. However, the hole generation/trapping process induced by cold carrier dominates the degradation of poly gate during CVS and HCS. The stress bias dependent positive charging, attributed to the hole generation/trapping, may complicate evaluation of the CVS and HCS and is not desirable for high-k stack. TiN metal gates show superior stress stability.

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QUESTIONS AND ANSWERS

Q: Is the electron hole generation expected to decrease with increasing temperature?
A: Yes, it would decrease at high temperature however; high temperature accelerates diffusion of generated hole to Si-interface degrading interface

Q: What do you think will be the charge trapping effects using FUSI gate electrode?
A: It might be similar with metal gate electrode but charge trapping is affected by mostly dielectric properties and possibly interface oxide quality.

Q: How heavily doped is the poly gate? All the way through?
A: 1e20 all the way through

Q: How do the holes drift? Is this hole diffusion or hole drift or something else? How do you distinguish between diffusion and drift? Please clarify.
A: We didn't study mechanism of hole migration through the dielectric to the bottom interface and therefore we can not distinguish between diffusion or drift processes.

Q: Do you think cold carriers can be the cause of PBTI?
A: We need to separate reversible cold carrier and irreversible cold carrier effects. At room temperature most degradations are reversible with poly-Si gate due to charge trapping. But, V_d dependence at high temperature allows to suggest electron-hole pair generated hole effects are not reversible at poly gate electrode. However metal gate might be different since it does not have e-h pair source. Therefore poly and metal gate effects need to be separated for PBTI.