# High Performance CMOS Devices on SOI for 90 nm Technology Enhanced by RSD (Raised Source/Drain) and Thermal Cycle/Spacer Engineering

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**Abstract**

We present enhanced 90 nm node CMOS devices on a partially depleted SOI with 40 nm gate length, featuring advanced process modules for manufacture including RSD (Raised Source/Drain), disposable spacer, final spacer for S/D doping and silicide proximity, NiSi, and thermally optimized MOL (Middle-of-Line) process. For the first time, we systematically designed silicide proximity in SOI and post-activation thermal cycles to improve series resistance and gate activation. This paper demonstrates decoupled effects of the individual performance boosters on drive currents and minimization of dopant deactivation, which resulted in dramatic improvement of drive currents by 11% to 19% (820 μA/um and 420 μA/um at Ioff = 40 nA/um with Vdd = 1.0V, for NFET and PFET, respectively), significant reduction in effective gate oxide thickness under gate inversion by ~1.2 Å and ~2.1 Å, for NFET and PFET, respectively, and an excellent inverter delay of less than 5.4 ps at Lgate of 40 nm.

## Introduction

As SOI CMOS devices are scaled down in 90nm technology node and below, design elements should be carefully selected and engineered to maximize device performance. First, the thickness of SOI layer is a critical parameter that limits drive currents and short channel characteristics. The SOI thickness in the S/D (source/drain) regions significantly affects the on-currents, while the body thickness on partially-depleted SOI limits the halo and extension doping and the short channel rolloff characteristics. Second, the thermal cycles and implant/anneal sequences need to be designed based on junction engineering and doping science. Dopant activation with spike RTA and deactivation during subsequent low temperature thermal cycles in the entire integration flow become extremely important in delivering high-performance devices at 40nm gate length. Third, the silicide on SOI devices and its proximity to the channel affect the series resistance and drive currents. These main design elements and process knobs are combined systematically to result in overall device performance enhancement.

## Silicide Proximity in SOI CMOS Design

In the pursuit of higher performance SOI CMOS, it becomes necessary for us to design optimal proximity of silicide tip to the channel and to the buried oxide interface. First, vertical proximity of the silicide to the buried oxide affects current crowding, doping in extension, and external resistance (FIG. 1 (a)), limiting the maximum on-currents. An RSD layer modulates the vertical proximity by increasing thickness of doped S/D regions, maintaining optimal body thickness. A thin body of partially depleted SOI combined with lower energy halo implants leads to better short channel rolloff characteristics. Second, lateral proximity of silicide tip to the channel region is also important. The final spacer size governs the lateral proximity of the silicide, which reduces overall series resistance, depending on the active doping level of S/D/extension regions. To maximize drive currents in a thin SOI (Tsi < ~70 nm), it is critical to optimize the spacer size and the RSD thickness, considering silicide thickness, body thickness, contact resistance, doping at silicide interface, and lateral doping encroachment into the channel.

### *(A) Vertical Proximity Effects: RSD*

When RSD process is integrated in a scaled CMOS technology, one needs to avoid adverse effects of additional thermal cycles for the Si selective epi process. The typical selective epi thermal budgets are high enough to cause TED (transient enhanced diffusion) of implanted halo dopants and boron penetration in the scaled devices during the epi growth, and degrade device performance such as short channel rolloff. Also, degradation of gate activation and its variability due to lateral overgrowth of epi on top of poly gate should be prevented [1, 2]. To achieve these goals, (i) extension and halo implantation should be done after the epi process, and (ii) gate poly should be capped when the epi is grown on S/D regions (FIG.1 (b)). By developing a novel disposable spacer integration scheme for RSD [2] sketched in FIG. 2, we have overcome the epi-related challenges.

FIG. 3 shows a cross-section of our RSD CMOS on SOI before silicidation. After $CoSi_2$ formation, the S/D regions thickened by RSD on a thin SOI significantly reduced source-



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to-drain series resistance in both NFET and PFET, as shown in FIG. 4. The changes in vertical proximity decreased the resistance caused by current crowding between the silicide and the buried oxide. FIG. 5 shows NFET and PFET drive currents are sizably improved by the RSD with $CoSi_2$.

***(B) Lateral Proximity Effects: Optimization of Final Spacer for Silicide and S/D Doping Proximity***

Closer lateral proximity of silicide tip to the channel reduces S/D series resistance further. In FIG. 6, by integrating a smaller final spacer, we made a significant improvement of Idsat over a large spacer in both NFET and PFET. The overlap capacitance was kept the same in this comparison. The improvement shown in FIG. 6 was made by combined effects of proximity of both silicide and self-aligned S/D doping to the channel. We observed such an improvement in drive currents and series resistance as long as the silicide does not encroach the extension junction.

In designing the final spacer size and integration sequence for S/D implant and silicide, we decoupled the effects between NFET and PFET, and between S/D junction and silicide, considering differences in S/D dopant species, dose/energy, and avoided lateral encroachment to effectively maximize on-currents for both NFET and PFET.

**NiSi and Dopant Deactivation: MOL Thermal Cycle**

For thin SOI devices, NiSi has a unique advantage over $CoSi_2$; Ni consumes a less amount of silicon than Co during silicidation for an equivalent sheet resistance. Thus, NiSi leads to an improved vertical proximity effect. FIG. 7 shows morphological differences between NiSi and $CoSi_2$. Besides the reduced thickness and roughness, it is likely that NiSi is formed better on narrower regions than $CoSi_2$. In FIG. 8, NiSi shows drastically lowered sheet resistance on narrower S/D regions of both NFET and PFET, in contrast to $CoSi_2$.

Application of NiSi requires much reduced thermal cycles for post-silicidation processes than $CoSi_2$ to avoid any defects associated with $NiSi_2$ formation and agglomeration. Thermal cycles for MOL processing which follows the silicidation should be optimized. In FIG. 9, the optimized MOL thermal cycles dramatically improved effective gate oxide thickness at gate inversion (Tinv) even with $CoSi_2$. With additional effects of NiSi, overall Tinv was reduced by ~1.2 Å and ~2.1 Å, reaching ~1.7 nm and ~2.1 nm for NFET and PFET, respectively. It is likely that additional deactivation was bypassed by NiSi process, which employs a single-step lower-temperature silicidation RTA, as opposed to typical two-step RTA processes for $CoSi_2$ formation at a higher temperature. The optimal thermal cycles for MOL and NiSi minimized deactivation of dopants in the gate, which successfully reduced gate depletion effects. Gate leakage did not increase significantly while the gate was further activated.

Dopant deactivation occurs in the S/D and the extension as well as in the gate. FIG. 10 (a) shows sheet resistance of an arsenic-doped extension region of an NFET as a function of junction depth (Xj); Once the extension dopants are activated by a high-temperature RTA, the sheet resistance stays low. After an additional short-time RTA at a low temperature (750°C), however, the activated arsenic is sizably deactivated even without diffusion. As a result, the sheet resistance increases significantly with a minimal change in extension junction depth. FIG. 10 (b) shows temperature dependence of deactivation in an $N^+$ S/D region in terms of relative change in sheet resistance as a function of temperature of a post-activation cycle that follows activation at 1000°C. Anneal time is also an important factor that determines the degree of deactivation at each temperature.

Deactivation in CMOS integration mostly occurs during low temperature thermal cycles after final dopant activation RTA, namely, silicidation and low temperature MOL cycles. With the optimal MOL thermal cycles, we eliminated or minimized the deactivation of dopants in the S/D and the gate that had been activated during final RTA at a higher temperature. Challenges in integration associated with the optimization were overcome. FIG. 11 shows that the MOL thermal cycle optimization tremendously improved drive currents by 11 and 19%, for NFET and PFET, respectively. It is a dramatic enhancement in our 90nm technology. In the comparison, off-currents and overlap capacitance Cov were kept the same. The deactivation effect is larger for PFET than NFET, since boron- and/or $BF_2$-doped S/D regions are more susceptible to the effect of the thermal cycle difference.

By the MOL thermal cycle optimization, we achieved a significantly enhanced ring speed and circuit performance. FIG. 12 exemplifies an inverter and NOR gate delays that are notably reduced. The improvement resulted solely from the thermal cycle engineering.

**Conclusion**

90 nm node SOI CMOS devices were shown with decoupled effects of advanced process modules. Systematic scaling of silicide proximity, doping confinement, and engineered thermal cycles successfully led to excellent performance including high drive currents and fast ring speed at a gate length of 40 nm.

**Acknowledgment**

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**References**

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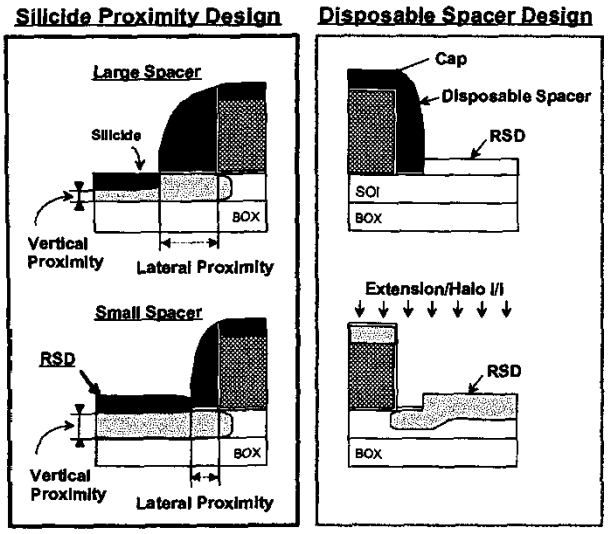
[2] H. Park, F. Assaderaghi, and D. Schepis, U.S. Patent #6,429,084 (2002).




(a) (b)

FIG. 1. (a) SOI CMOS design concept of vertical and lateral proximity of silicide to the channel and to the buried oxide interface; (b) Design of disposable spacer for RSD integration.

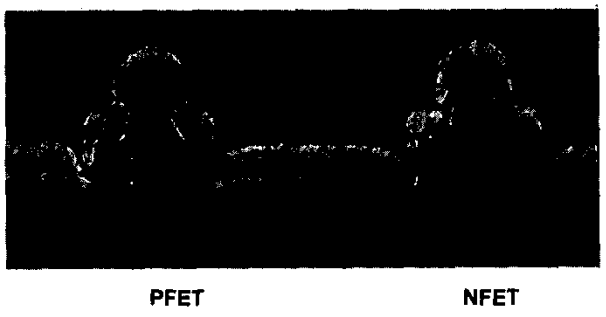



FIG. 3. RSD CMOS devices after final spacer formation.

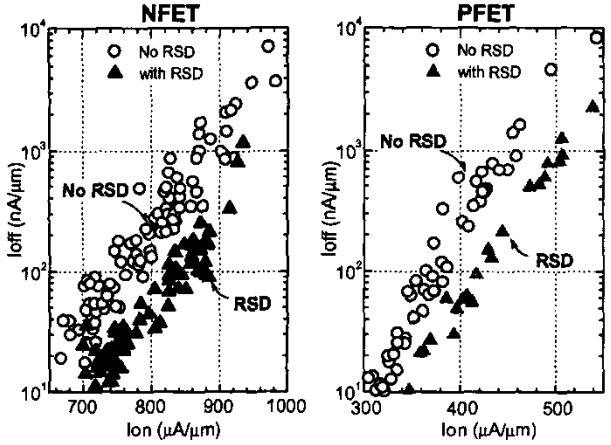



FIG. 5. Effects of RSD on Idsat vs. Ioff (Vdd=1.0V); with $CoSi_2$.

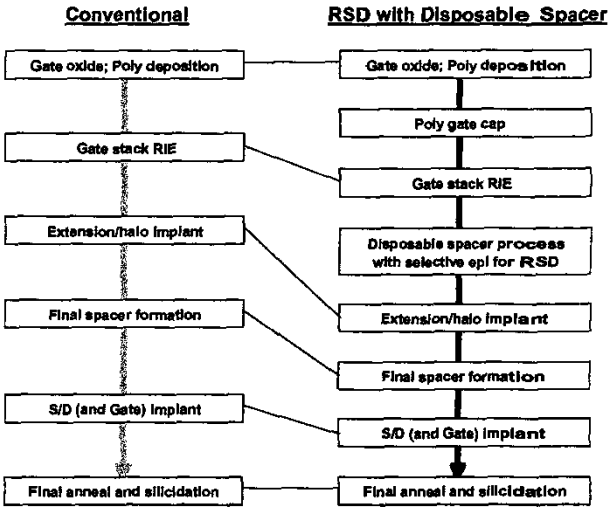



FIG. 2. A schematic flow of RSD with disposable spacer integration compared with a conventional CMOS process.

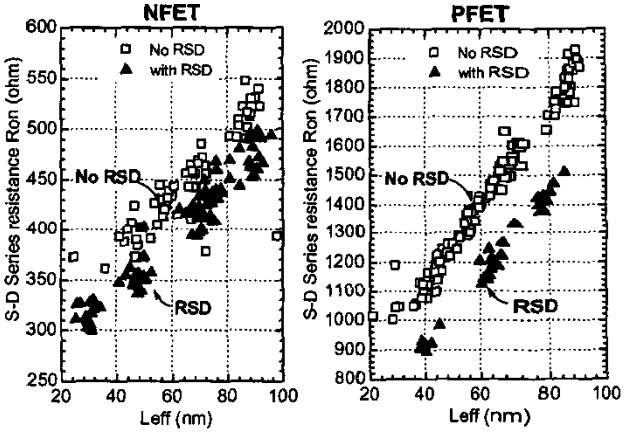



FIG. 4. RSD effects on source-to-drain series resistance under a gate overdrive condition; with $CoSi_2$.

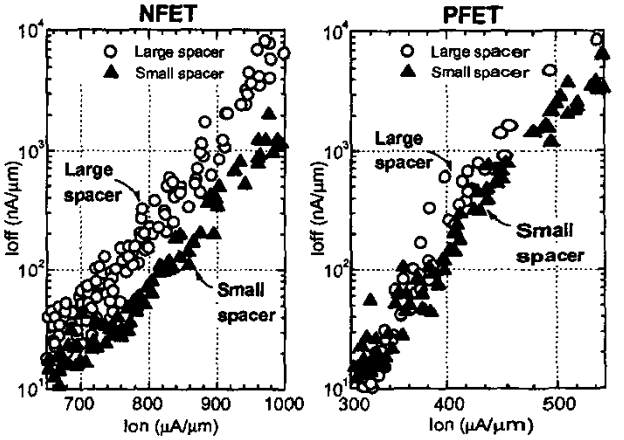
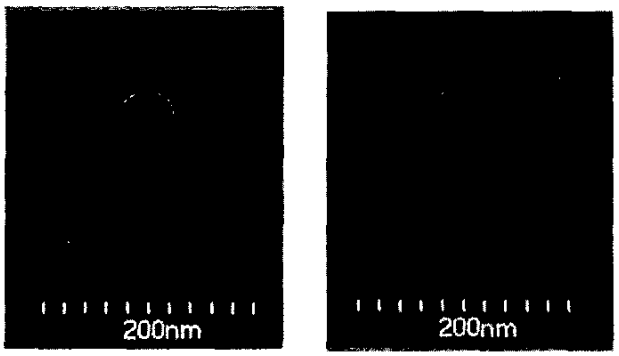



FIG. 6. Effects of spacer scaling on Idsat vs. Ioff (No RSD).




(a) $CoSi_2$ (b) NiSi

FIG. 7. SEM images of a non-RSD device with (a) $CoSi_2$ and (b) NiSi.

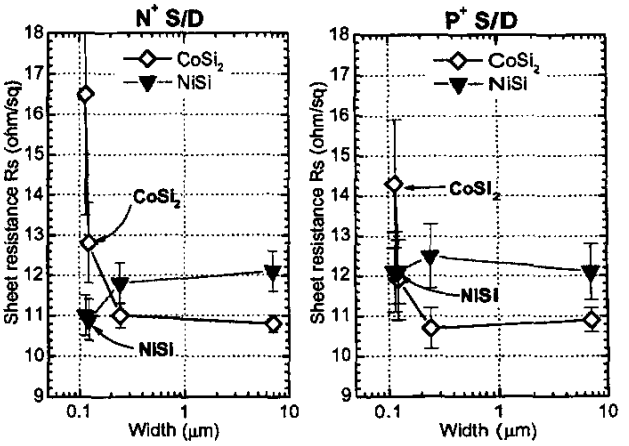



FIG. 8. Dependence of Rs on width of $N^+$ and $P^+$ S/D regions silicided with $CoSi_2$ and NiSi.

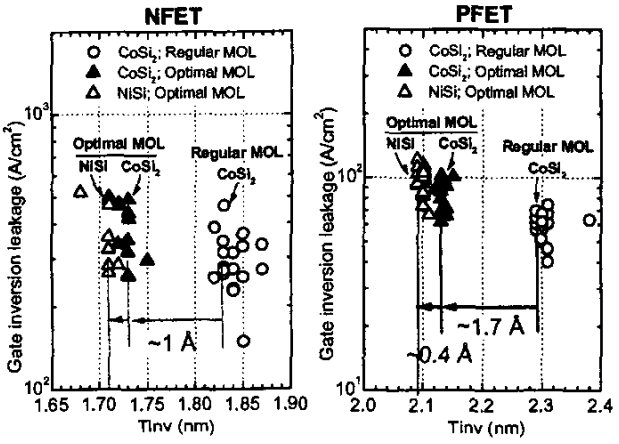
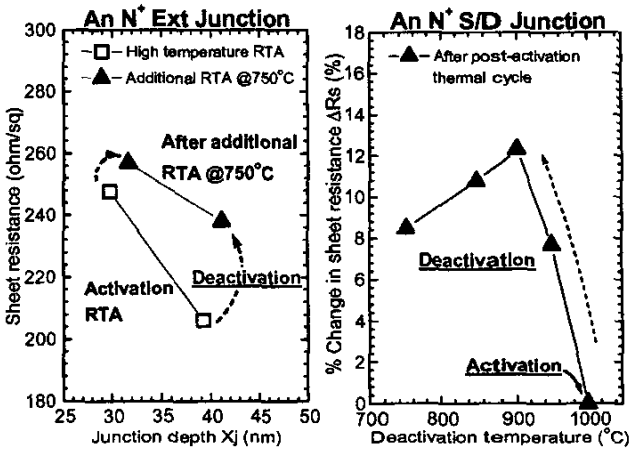



FIG. 9. Effects of MOL thermal cycle optimization and silicidation on effective gate oxide thickness under gate inversion condition (Tinv) and gate tunneling current.




(a) (b)

FIG. 10. (a) Deactivation anneal effects on sheet resistance vs. junction depth for an unsilicided NFET junction; (b) Changes in Rs of NFET S/D regions vs. post-activation thermal cycles.

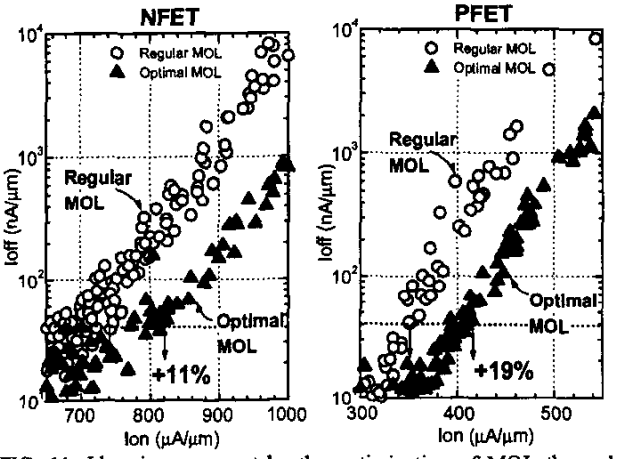



FIG. 11. Idsat improvement by the optimization of MOL thermal cycles (No RSD; the same Cov; Vdd=1.0V).

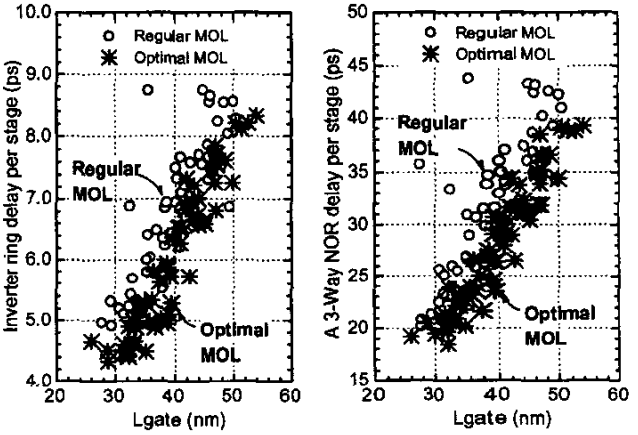



FIG. 12. MOL thermal cycle effects on delay per stage of an inverter ring and a 3-way NOR at Vdd=1.0V.