Investigation of Random Telegraph Noise in Gate-Induced Drain Leakage and Gate Edge Direct Tunneling Currents of High-$k$ MOSFETs

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Abstract—Random telegraph noise (RTN) in gate-induced drain leakage (GIDL) and gate edge direct tunneling (EDT) leakage currents under GIDL bias conditions was characterized in MOSFETs with a high-$k$ gate dielectric for the first time. The RTNs were analyzed through systematic measurement and calculation. The results indicate that a high-current state in a GIDL current can be attributed to electron capture due to thermal emission. However, electron emission from a trap was mainly affected by gate bias. Both capture and emission times in the RTN of the EDT current had gate bias dependence. Moreover, multilevel RTN waveforms were detected in a device, and our analysis indicated that the multilevel RTN is the result of the combination of the RTNs of the GIDL and EDT currents. The analysis also indicated that two independent traps in the high-$k$ gate dielectric can produce a four-level RTN in the GIDL current. This paper provides the fundamental physics required to understand such leakages in nanoscale MOSFETs and devices that utilize band-to-band tunneling.

Index Terms—Edge direct tunneling (EDT), gate-induced drain leakage (GIDL), high $k$, random telegraph noise (RTN).

I. INTRODUCTION

Random telegraph noise (RTN) caused by carrier capture and emission at electron traps has been studied in MOSFETs [1]–[4]. The RTN in carbon nanotube FETs has also been studied [5], [6]. Most of them have been characterized for FETs with a SiO$_2$ gate dielectric. Recently, the RTN in high-$k$ FETs has also been studied [7], [8]. Drain current ($I_D$) fluctuations as a result of single-hole trapping in HfSiON high-$k$ gate dielectric p-channel FETs (pFETs) have experimentally been investigated and compared with those in SiO$_2$ gate dielectric pFETs [7]. In addition, the RTN in the gate leakage current of n-channel FETs (nFETs) with a HfSiO high-$k$ gate dielectric has been reported [8]. In that work, the authors mentioned that electrons in the body are able to tunnel directly into the gate dielectric and move to the gate. However, electron tunneling from the drain and/or the source to the gate had not been considered. Until now, most studies on RTN have focused on the channel current of MOSFETs, and the RTN in the gate-induced drain leakage (GIDL) current of high-$k$ or SiO$_2$ gate dielectric FETs has not previously been reported. Nowadays, understanding band-to-band tunneling (BTBT), which is the main physical origin of GIDL, is important in dynamic random access memory (DRAM) cells [9], flash memory cells [10], and tunneling FETs (TFETs) [11]. Since GIDL in DRAM cells is a major component of the total leakage [9], it needs to be well understood. Furthermore, nonvolatile memory cells that utilize the GIDL current have been reported and have shown excellent performance [10]. Recently, TFETs that achieve sub-60-mV/dec swings by using BTBT have been reported [11]. Considering these advances, it was timely to study and understand the RTN in the GIDL current. In measuring GIDL, there may be a concurrent gate edge direct tunneling (EDT) leakage current that flows between the gate and the drain (or the source) overlapped by the gate [12], [13]. The EDT of electrons from the gate to the underlying n-type drain extension has been examined in off-state n-channel MOSFETs having a ultra-thin gate oxide [13]. EDT is more pronounced for thin gate oxides, and EDT affects the GIDL current measured at the drain terminal. Therefore, it is imperative to check the contribution from EDT under GIDL bias conditions.

In this paper, the RTN in $I_D$, $I_B$, and $I_G$ of HfSiON high-$k$ gate dielectric nFETs is investigated through systematic experimentation and calculation. First, we elucidate the two-level RTN in the drain current by GIDL only or EDT only in terms of capture probability with gate bias, trap depth, and temperature. In addition, we characterize the multilevel RTN in the drain current and physically analyze the electron capture and emission process. In this paper, the drain current is a GIDL and/or EDT current but is not a channel current.

II. DEVICE FABRICATION

For the experimental work, we used nFETs with a high-$k$ gate dielectric. The HfSiON high-$k$ dielectric was deposited using an atomic layer deposition (ALD) method after chemical cleaning to form a SiO$_2$ interfacial layer (IL), as previously described [14]. The concentration of HfO$_2$ used during
deposition was approximately 20%. The high-k dielectrics were nitrided using a plasma nitridation process and annealed to densify the film. Then, TiN electrodes were deposited using an ALD method. The resulting gate stack comprised a TiN gate electrode, a 2.7-nm HfSiON high-k layer, and a SiO2 IL. The equivalent oxide thickness of the IL was ~0.6 nm. After the gate stack process, a CMOS process that included a lightly doped drain with halo implantation, 1000 °C rapid thermal annealing, CoSi2, and a Ti/TiN/W contact scheme were used to fabricate well-controlled short-channel devices. The transistors investigated had a gate width of 10 μm and a gate length of 0.06–0.5 μm.

III. RESULTS AND DISCUSSION

RTN fluctuations in \( I_D, I_B, \) and \( I_G \) were measured under GIDL bias conditions. These are measured one after the other due to the limitation for measuring three currents at the same time and plotted to the same time interval. The \( V_G, V_D, \) and \( V_B \) that were applied were \(-0.3, +1.5, \) and 0 V, respectively, for nFETs for the measurement of GIDL. We first checked the effect on GIDL from the n+-p junction diode (n+ drain to p-body) and determined that the junction leakage measured at a \( V_D \) of 1.5 V and a \( V_B \) of 0 V was negligible (< 10 pA) compared to the GIDL current (> 50 nA).

During GIDL measurement, an electron may be detrapped or trapped. Such trapping would take place inside the gate dielectric on the drain that is overlapped by the gate region. The trapping and detrapping of an electron can produce variation in the surface potential in the n+ drain overlapped by the gate and thus result in RTN in the GIDL current. Such RTN in GIDL currents can simultaneously be detected in both drain and body currents. Under GIDL bias conditions, the high electric field in the dielectric between the gate and the drain produces the gate leakage current. If there is an active trap along the leakage path, electrons can be trapped or detrapped, which simultaneously produces RTN in \( I_D \) and \( I_B \).

Fig. 1(a) and (b) shows the measured \( I_D, I_B, \) and \( I_G \) under GIDL bias conditions of \( V_{GS} = -0.3 \) V, \( V_{GB} = -0.3 \) V, and \( V_{DS} = +1.5 \) V in nFETs. The gate lengths \( L_g \) in Fig. 1(a) and (b) are 0.3 μm and 0.08 μm, respectively. The \( \Delta I_G, \Delta I_D, \) and \( \Delta I_B \) terms represent the current fluctuations due to the RTN in \( I_G, I_D, \) and \( I_B \), respectively. \( I_D \) is equal to the sum of \( I_B \) (consisting mainly of GIDL current) and \( I_G \) (the EDT leakage current). Most of the \( I_G \) is the result of the tunneling current that flows between the gate and the drain overlapped by the gate, because \( V_{GD} \) (~1.8 V) is much larger than \( V_{GS} \) (~0.3 V) and \( V_{GB} \) (~0.3 V). The tunneling currents from the gate to the source and to the channel are less than 10 and 20 pA, respectively.

In Fig. 1, two samples in the same wafer showed different characteristics. In Fig. 1(a) (sample 1), \( I_D \) and \( I_B \) show RTN, and the \( \Delta I_D \) resulting from the RTN is almost the same as \( \Delta I_B \). However, there is no RTN in \( I_G \). Therefore, it appears that GIDL is a main cause of the RTN. Electron-hole pairs are generated in the n+ drain overlapped by the gate; the electrons go to the drain terminal, and the holes move to the body along the surface of the drain. Here, a trap with a captured electron increases the vertical electric field in a localized surface area and increases GIDL as a result, which means that the high current level in the RTN waveform reflects an electron-captured state. Thus, a low current level in the RTN waveform can be explained by electron emission. A trap with a detrapped electron in a gate dielectric reduces the vertical electric field, resulting in a decrease in the GIDL current. Thus, the trapping and detrapping of an electron produces RTN in the GIDL current.

In Fig. 1(b) (sample 2), \( I_D \) and \( I_G \) show RTN, and the \( \Delta I_D \) is nearly the same as \( \Delta I_G \). However, there is no RTN fluctuation in \( I_B \), which indicates that there is no active trap to generate RTN in the GIDL current. This result suggests that a trap in the gate dielectric can trap and detract electrons while the EDT current is flowing, which is the main cause of RTN. Here, a trap with a captured electron hinders the electron flow from the gate in a localized area and slightly decreases \( I_G \), which leads to the low current level in RTN waveform. The detrapping of the electron (electron emission) results in the \( I_G \) returning to an undisturbed value, which is the high current level in RTN waveform. The trapping and detrapping process generates RTN in \( I_G \) and \( I_D \). In Fig. 2(a), the dependence of capture time \( (\tau_c) \) and emission time \( (\tau_e) \) on the gate voltage in samples 1 and 2 of Fig. 1 is shown. In sample 1, \( \tau_e \) is independent of the gate voltage because an electron from the valence band of the high-k dielectric is thermally emitted to a detrapped trap. However, the \( \tau_e \) of sample 1 increases with increasing \( V_{GS} \), which indicates that electron detrapping becomes more difficult as \( V_{GS} \) increases. This can be explained using two energy band diagrams (see Fig. 2 insets) to depict the behavior of electron detrapping with \( V_{GS} \). Generally, a trap energy \( (E_T) \) that is similar to Fermi energy \( (E_F) \) actively contributes to low-frequency noise.

Now, assume that \( E_T \) is slightly higher than \( E_F \) when the \( V_{GS} \) is low (sample-1 left inset). As \( V_{GS} \) increases, \( E_T \) becomes slightly lower than \( E_F \) (sample-1 right inset). Thus,
with increasing $V_{GS}$, the probability of detrapping of a captured electron decreases because of a decrease in the $E_T - E_F$, which results in an increasing $\tau_e$. In sample 2, $\tau_e$ increases with increasing $V_{GS}$, which means that the captured electrons are mainly detrapped not by thermionic emission but by the electric field. It is very difficult to emit an electron from a trap to the conduction band of a high-$k$ dielectric because $E_{C, high-k} - E_T$ is much larger than $E_T - E_{V, high-k}$ in our samples. Here, $E_{C, high-k}$ and $E_{V, high-k}$ represent the conduction band and valence band energies of the high-$k$ dielectric, respectively. As $V_{GS}$ increases, $E_T - E_F$ slightly decreases, as shown in the sample-2 inset, which, in turn, decreases the probability of electron emission from a trap to the drain. In contrast, the $\tau_c$ of sample 2 decreases with increasing $V_{GS}$. Then, $E_T - E_F$ slightly decreases, as shown in the $\tau_e$ explanation of sample 2, which, in turn, increases the capture probability of the electron from the drain to a trap. Fig. 2(b) shows the $\ln(\tau_c/\tau_e)$ of the RTN in samples 1 and 2 versus $V_{GS}$. The trap depth ($x_T$) can be obtained by using a conventional method [2] and by considering the different dielectric constants of the SiO$_2$ IL and the HfSiON high-$k$ gate dielectric [15]. Since $x_T$'s for samples 1 and 2 are 1.3 and 0.78 nm, respectively, both traps are located in the HfSiON layer. The insets show the samples’ energy band diagrams, including $x_T$.

Fig. 3(a) and (b) shows RTN waveforms of $I_D$’s for samples 1 and 2, respectively, in a time domain as a parameter of temperature ($T$). Here, the same bias as that in Fig. 1 is applied to samples 1 and 2. As $T$ increases, both $I_D$ and $\Delta I_D$ increase because the GIDL currents are increased due to the trap-assisted generation of electron-hole pairs [16] and direct tunneling gate currents are increased due to the
thermionic-type emission current [17]. Capture and emission events happen more frequently with increasing $T$ in both samples because the electrons can easily surpass the barrier for capture and emission. It is interesting to note that the high-current portion of RTN in GIDL (sample 1) significantly increases with increasing $T$. As mentioned in the explanation of Fig. 2(a), thermionic emission dominates the capture process in a trap concerning the GIDL current. As $T$ increases, the thermionic emission from the valence band of the gate dielectric becomes easier; thus, a trap captures an electron more frequently, which leads to the larger portion of high-current state in sample 1.

Differently, in sample 2, the ratio of high- and low-current states is similar with $T$ because both $\tau_c$ and $\tau_e$ are strongly dependent on $V_{GS}$. Fig. 3(c) shows the dependence of $\tau_c$ and $\tau_e$ on $T$, and the activation energies extracted from these data. For a trap in sample 1, the capture activation energy (0.28 eV) is much larger than that (0.11 eV) for emission. In contrast, although the trap in sample 2 has larger capture activation energy (0.24 eV) than that (0.19 eV) for emission, the energy difference is relatively small.

In Fig. 4(a) and (b) shows fluctuations in waveforms over time in $I_D$, $I_B$, and $I_G$ in nFETs under the same GIDL bias conditions as shown in Fig. 1. These are measured one after the other due to the limitation for measuring three currents at the same time and plotted to the same time interval. $L_g$’s in Fig. 4(a) and (b) are 100 and 75 nm, respectively. The device (sample 3) in Fig. 4(a) has RTN in both GIDL and EDT currents because $I_G$ and $I_B$ exhibit a two-level RTN. Since $I_D$ consists of the sum of $I_G$ and $I_B$, we can expect a four-level RTN in $I_D$. However, a three-level RTN pattern is depicted in $I_D$. The $\Delta I_G$ is nearly the same as $\Delta I_B$ at the $V_{GS}$ of $-0.3$ V, which is why the three-level RTN is observed. If we change $V_{GS}$, then the $\Delta I$’s for both currents would be different, resulting in a four-level RTN. Note that the RTN in $I_B$ changed more frequently than that in $I_G$ and that the RTN in $I_D$ reflects the waveforms in $I_G$ and $I_B$.

In Fig. 4(b), the nFET (sample 4) shows four levels of RTN in both $I_B$ and $I_D$ but no RTN in $I_G$. Because there is no RTN in $I_G$, there is no trap for the RTN in the EDT current. The four-level RTN in sample 4 is attributed to the presence of two independent traps that affect the GIDL current. The $\Delta I$’s in $I_D$...
shows the vertical positions of the two traps.

are nearly the same as those in $I_B$. In both $I_D$ and $I_B$, the $\Delta I$ of one trap (trap 1; $\Delta I = 0.5$ nA) is larger than that of the other trap (trap 2; $\Delta I = 0.35$ nA). The complex RTN observed in Fig. 4 was analyzed by examining sample 3 in more detail.

Fig. 5(a) shows the dependence of $\tau_c$ and $\tau_e$ on $V_{GS}$ for the RTNs in $I_B$ and $I_G$ of sample 3. For the RTN of $I_B$ (the mainly GIDL current) of sample 3, $\tau_c$ is independent of the $V_{GS}$, as shown in the left panel of Fig. 5(a), thus indicating that an electron is captured in the trap by thermionic emission, as was also indicated in the left panel of Fig. 2(a). Furthermore, the left panel of Fig. 5(a) shows that $\tau_c$ increases with increasing $V_{GS}$; such behavior can be explained by the same rationale as that used for sample 1. The right panel of Fig. 5(a) shows that the behavior of $\tau_e$ and $\tau_c$ with $V_{GS}$ for the RTN of the EDT current ($I_G$) is similar to that in sample 2 in which RTN is only present in the EDT current. Fig. 5(b) shows the ln($\tau_c$/\tau_e) versus $V_{GS}$ for the RTNs in $I_B$ and $I_G$ of sample 3. The $\chi_T$'s for the traps were extracted using the method in [2] and [15], and the results show that the trap responsible for the RTN in GIDL is located in the high-$k$ dielectric layer ($\chi_T = 0.783$ nm). The IL includes the trap ($\chi_T = 0.05$ nm) that affects the RTN in the EDT current. The insets in Fig. 5(b) show energy band diagrams, including $\chi_T$. From the results of sample 3 in Fig. 4(a), which shows RTNs in the GIDL and EDT currents, we understand that the RTN in $I_D$ comes from a combination of the RTNs in the GIDL and EDT currents. Fig. 5(c) shows the $\Delta I$’s in the RTNs of the GIDL and EDT currents versus $V_{GS}$. At a $V_{GS}$ of $-0.3$ V, both RTNs are similar, which produces a three-level RTN in $I_D$, as was also shown in Fig. 4(a). As the $V_{GS}$ increases, the $\Delta I$ of the GIDL current decreases more rapidly compared to the $\Delta I$ of the EDT current. At $V_{GS}$ values other than $-0.3$ V, the $\Delta I$’s in both RTNs are different, which results in a four-level RTN.

Fig. 6 shows ln($\tau_c$/\tau_e) versus $V_{GS}$ for the RTNs in $I_B$ or $I_D$ of sample 4, which had two independent traps that were responsible for producing the four-level RTN in the GIDL current. The behavior of $\tau_c$ and $\tau_e$ versus $V_{GS}$ in the RTN for each trap is quite similar to that for the RTN in the GIDL current shown in Fig. 2(a). The extracted $\chi_T$‘s for traps 1 and 2 are 0.55 and 1.164 nm, respectively. The inset in Fig. 6 schematically

IV. CONCLUSION

Two-level and four-level RTNs have been measured in the GIDL current for the first time in MOSFETs containing a HISON high-$k$ gate dielectric and have been analyzed through experimental measurement and calculation. Under GIDL bias conditions, the EDT leakage current flows through the gate dielectric between the gate and the drain overlapped by the gate and produces RTN if there is a trap within the dielectric. The mechanism of carrier capture and emission for the RTNs in both GIDL and EDT currents have been physically analyzed, and multilevel RTNs, which come from the RTNs in the GIDL and EDT currents of a FET, have been investigated. This paper will improve the understanding of devices that utilize the BTBT process and help the analysis of leakage currents in future devices.

REFERENCES


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