Thermally robust dual-work function ALD-MN_x MOSFETs using conventional CMOS process flow

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Abstract

Thermally stable dual work function metal gates are demonstrated using a conventional CMOS process flow. The gate structure consists of poly-Si/metal nitrides (MN_x)/ SiON (or high-k)/Si stack with atomic layer deposition (ALD)-TaN_x for the NFET and ALD-WN_x for the PFET. Much enhanced drive current (I_d) and transconductance (G_m) values, and reduced off current (I_{off}) characteristics were attained with ALD-MN_x gated devices over control poly-Si and PVD-MN_x devices within controllable V_t shifts. Excellent scalability of dual work function MN_x/high-k gate stack was demonstrated: the EOT was down to 6.6Å with low leakage in a low thermal budget device scheme.

Introduction

With aggressive scaling of CMOS devices, it is imperative to replace poly-Si gates by metal gates to eliminate poly-depletion. The most desired metal gates should possess work functions close to Si band edges for CMOSFETs. More importantly, these metal gates should be thermally stable to employ a conventional process flow for fabrication; however, it is extremely challenging to identify two thermally stable metal gates with the correct work functions [1,2]. Furthermore, the method of preparing the metal gates is critical due to process induced damage [3] and/or Fermi level pinning [4]. In this paper, for the first time, we report the successful fabrication of N- and PMOSFETs using thermally stable Poly-Si/ALD-MN_x (TaN_x for NFET and WN_x for PFET) stacks by conventional CMOS process flow with a thermal budget up to 1000 °C for 5s.

Experimental Results and Discussion

Metal gate films (<15nm) were prepared by ALD using a Ta-metal organic precursor and NH_3 for TaN_x and a W precursor and NH_3 for WN_x. Sputtered (PVD) TaN_x and WN_x devices were also prepared for comparison. This was followed by conventional CMOS processing: deposition of poly-Si, gate patterning, and activation anneal performed at 1000 °C for 5s (Table 1). ALD-TiN_x was also evaluated as a midgap work function material. For gate dielectrics, Si-oxynitride (10-15Å) and HfO_2 (20-30A)/SiO_x were used. The equivalent oxide thickness (EOT) was obtained by quantum mechanical extraction.

Benefit of Poly/MN_x stack: We found that employing a poly/ALD-MN_x gate stack over pure ALD-MN_x gate can enhance the thermal stability of ALD-MN_x (TiN_x, TaN_x, WN_x). Fig. 1 shows improved thermal stability of poly/ALD-TiN_x gate stack compared to TiN_x stack only, which is corroborated by a more stable C-V curve and two orders of magnitude lower gate leakage current. Moreover, we further observed that ALD-TaN_x showed better thermal stability. Fig. 2 represents TEM images of poly/ALD-MN_x(TiN_x, TaN_x)/SiON/Si stack, where non-uniform gate oxide was observed with TiN_x presumably due to the uncontrolled columnar grain growth at elevated temperature. However, as-deposited ALD-TaN_x showed an amorphous structure (not shown), and uniform crystallization after high temperature anneal, resulting in 70X leakage current reduction compared to ALD-TiN_x stack (Fig. 3).

NMOSFET of Poly/TaN_x stack: Fig. 4 shows the Id-Vg curves of poly/TaN_x gated NMOSFET and a control n+ poly-Si gate using 15Å SiON for both devices. The threshold voltage (V_t) shift is about 150 mV for the TaN_x sample with respect to poly-Si. The drive currents of TaN_x gated devices are 20% higher than the control poly-Si sample at the same (Vg-Vt) points. This result is consistent with the higher G_m of TaN_x devices, where the peak G_m values are 15 to 20% higher at both Vds=0.05V and 1.2V. Both devices show comparable subthreshold slope (S_t) values at about 70mV/dec, indicating comparable and good interface quality for the two devices. Interestingly, the I_{off} values for TaN_x gated device are significantly lower than those for poly-Si gated devices, which suggests improved short channel effects due to the smaller T_{inv} of TaN_x devices. The improvement of drive current is mostly from the T_{inv} gain, and no mobility degradation is observed.

PMOSFET of poly/WNx stack: The work function and thermal stability data of the poly/WN_x stack are shown in Figs 5 and 6. ALD-WN_x exhibited a work function of ~5.1 eV for PFET and poly/WN_x stack showed enhanced thermal stability up to 1000 °C as manifested by in-situ synchrotron x-ray analysis (Fig.6). Fig. 7 shows the Id-Vg curves of PMOSFETs gated with poly/ALD-WN_x and p^+ poly-Si. The V_t shift is less than 100 mV compared to the poly-Si control devices, indicating feasibility of ALD-WN_x as a PMOSFET metal gate candidate. The WN_x PMOSFETs also exhibited much higher drive currents and G_m than the p^+ poly-Si gate. The improvement in drive current comes from the T_{inv} gain and negligible mobility degradation. The similar S_t of WN_x stack to the control sample indicates a low interface trap density for FETs prepared by ALD method. Fig. 8 reveals another reason for the superiority of ALD-MN_x as a metal gate preparation method. The poly/PVD-WN_x stack resulted in three orders of magnitude higher I_{off} and lower G_m values compared to poly/ALD-WN_x due to process induced plasma damage inherent to PVD method [3] and large V_t shift (-500 mV). We also observed comparable device enhancement with 12Å-thick SiON using poly/ALD-WN_x stack.

Poly/MN_x/HfO_2: Fig. 9 shows the C-V and J-V characteristics of poly/TaN_x/HfO_2/SiO_x/Si MOS capacitors. Robust thermal stability is shown on high-k materials with ALD-TaN_x, while PVD-TaN_x displayed 100X higher gate leakage current for a similar EOT range due to the same reason as above (Fig. 8). The low EOT (7.7A) and leakage current (~3×10^{-4} A/cm^2) of poly/ALD-TaN_x/HfO_2/SiO_x stack after RTA at 1000 °C-5s is promising for the NFET. Fig. 10 displays the scalability data of ALD-MN_x/HfO_2 material for low thermal budget devices. We have achieved sub-mA/cm^2 range leakage current near the operating voltage for ALD-TaN_x with an EOT as low as 6.6Å, and for ALD-WN_x with an EOT about 8Å, for 45 nm technology node and beyond.

Conclusion

In summary, thermally stable ALD-MN_x MOSFETs were successfully demonstrated using ALD-TaN_x for the NFET and ALD-WN_x for the PFET with comparable V_t, significantly higher drive current and G_m (~20%), negligible mobility degradation, and reduced I_{off} compared to the control poly-Si gate. The improved device performance was primarily ascribed to elimination of poly-depletion, good interface quality and comparable mobility. We also demonstrated the scalability of MN_x/high-k gate stack down to an EOT~7.7Å for conventional CMOS flow and to 6.6Å for a low thermal budget device.

References

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- STI/CMOS Channel I/I
- SiON (10-15A), HfO_2(20-30A)
- Electrodes: **ALD**/PVD-MN_x
  MNx: TaN_x, TiN_x, WN_x
- Poly-Si dep/ Gate Patterning
- LDD/Halo I/I (CMOS)
- Spacer Formation and S/D I/I
- Activation Anneal (1000C-5s)
- Co-Salicidation
- Conventional ILD/Contact scheme
- Metal 1 Patterning/FGA

Table 1. A schematic of conventional MOSFET process flow.

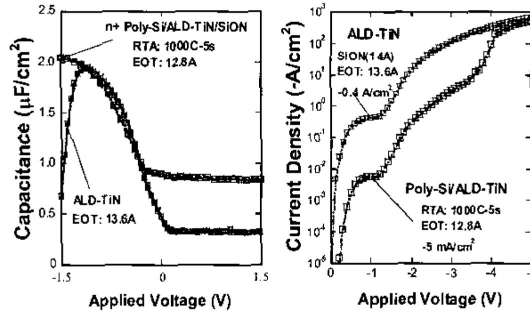

Fig. 1. (a) C-V and (b) J-V characteristics of ALD-TiN_x as a function of capping poly-Si. Poly/ALD-TiN_x structure improved the thermal stability of gate stack against conventional MOSFET process flow.

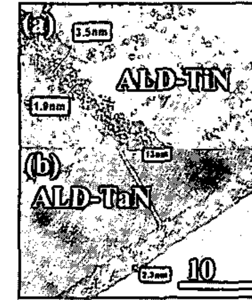

Fig. 2. HRTEM images of poly/ALD-MNx/ SiON/Si structure after RTA of 1000C-5s; (a)ALD- TiN_x and (b)ALD-TaN_x.

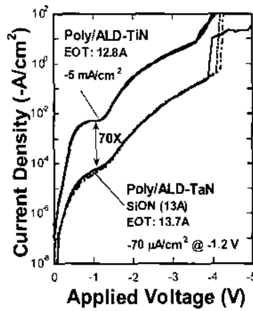

Fig. 3. J-V characteristics of poly/ALD-MNx/SiON(13A)/Si structure after RTA of 1000C-5s.

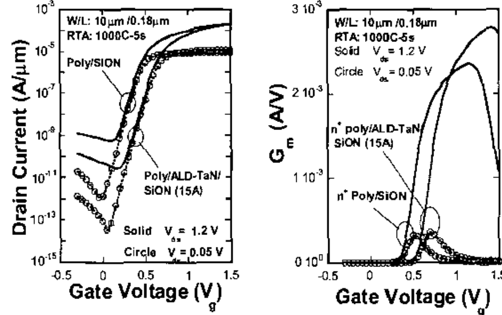

Fig. 4. (a) Id-Vg and (b) G_m-Vg characteristics of NMOSFETs. The peak G_m of TaN_x is ~20% higher than that of poly-Si gate.

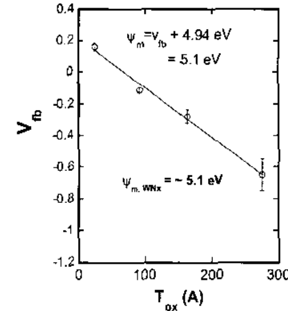

Fig. 5. Work function extraction of ALD-WN_x, exhibiting the PFET work function feasibility.

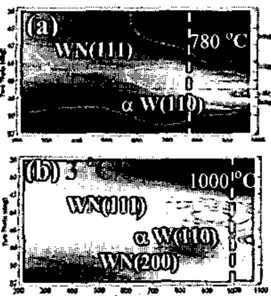

Fig. 6. Increased dissociation temperature of poly/WNx structure up to 1000C as evidenced by synchrotron XRD; (a) no poly-Si cap (b) poly-Si (30nm) cap.

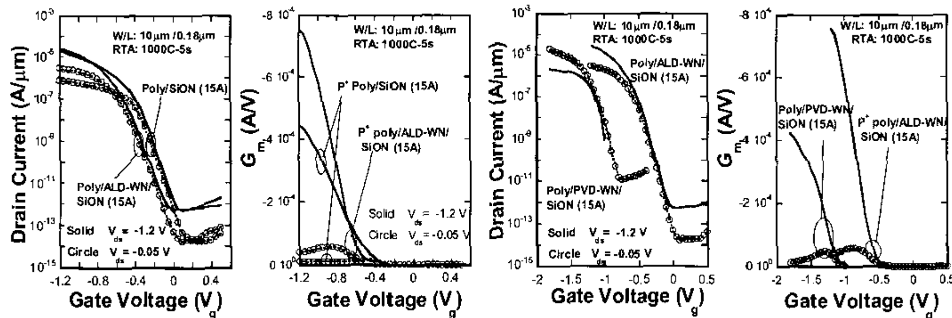

Fig. 7. Characteristics of poly/ALD-WN_x/SiON/n-Si PMOSFET showing (a) Id-Vg and (b) Gm-Vg curves after conventional CMOS process flow.

Fig. 8. (a) Id-Vg and (b) Gm characteristics of poly/WNx/SiON as a function of WNx deposition method. ALD-WNx showed 2 order of magnitude lower I_{off} and higher G_m.

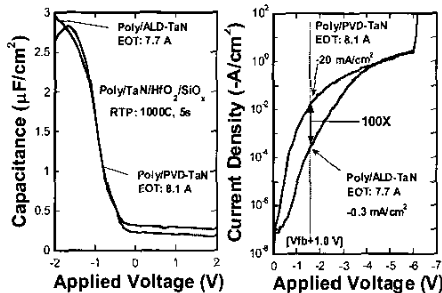

Fig.9 (a) C-V and (b) J-V characteristics of Poly/TaN_x/HfO2/ SiOx/p-Si MOS capacitors. ALD-TaN_x reduced the gate leakage current about 2 orders of magnitude with similar EOT.

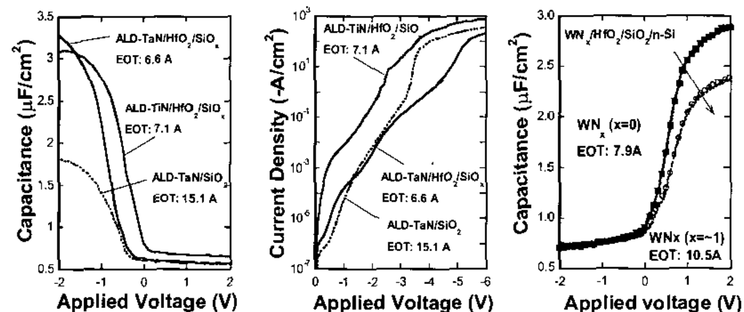

Fig.10. Scalability of ALD-MN_x for low thermal budget device scheme.