Hot carrier degradation in HfSiON/TiN fin shaped field effect transistor with different substrate orientations

Chadwin D. Young, a) Ji-Woon Yang, Kenneth Matthews, b) Sagar Suthram, c) Muhammad Mustafa Hussain, Gennadi Bersuker, Casey Smith, Rusty Harris, d) Rino Choi, e) Byoung Hun Lee, and Hsing-Huang Tseng
SEMATECH, 2706 Montopolis Drive, Austin, Texas 78741
(Received 10 June 2008; accepted 29 December 2008; published 9 February 2009)

Hot carrier injection (HCI) degradation is evaluated for n-metal oxide semiconductor (MOS) and pMOS high-k-fin shaped field effect transistor with (100) and (110) sidewall surface orientations. It was found that impact ionization at the source, in addition to the traditional drain side enhances HCI degradation for the \( V_g = V_d \) condition. The degradation increases with decreasing fin length, with negligible dependence on substrate orientation. © 2009 American Vacuum Society. [DOI: 10.1116/1.3072919]

I. INTRODUCTION

For future technology nodes below 45 nm, engineered high mobility channels and/or alternative devices such as fin shaped field effect transistors (FinFETs) will be required in order to meet the high performance requirements. In addition, substrate surface orientation has also demonstrated performance enhancements.1,2

Because of their exceptional scalability and relatively simplistic fabrication, FinFETs have become a plausible solution for improved performance in future devices. However, the three-dimensional (3D) device structure still requires additional process complexities as compared to conventional complementary metal oxide semiconductor (CMOS) technology. The fabrication process can construct fins with different sidewall channel orientations. Surface orientation or fin structure may be more susceptible to degradation during stress. Possible causes could be due to more Si interface bonds available for bond breakage,3 or structural properties that impact reliability differently than planar devices. In addition, these devices will most likely require high-k gate dielectrics and metal electrodes which also impact reliability differently than conventional planar SiO2 CMOS devices. In this work, hot carrier injection (HCI) stress is executed and evaluated on n-metal oxide semiconductor (MOS) and pMOS high-k FinFETs with (100) and (110) sidewall surface orientations to understand the impact that fabrication process effects have on sidewall orientation and FinFET device structure when subjected to HCI stress.

II. EXPERIMENT

The starting materials for this work are (100) silicon-on-insulator wafers with an ~90 nm silicon layer and ~125 nm buried oxide. The silicon body is slightly p type (2 \( \times 10^{15} \) /cm\(^3\)) without any additional channel doping. Conventional 193 nm dry lithography with numerical aperture of 0.7 was utilized to pattern (110)[110] and (100)[100] fin arrays at 200 nm pitch perpendicular and 45° to the notch direction, respectively. Prior to gate stack deposition, a novel annealing and cleaning sequence was utilized to smooth the fin sidewalls and thereby reduce mobility degradation due to surface scattering.4 The gate stack for these sub-20-nm width fins consists of 1 nm SiO2/2 nm HfSiON/TiN/poly-Si and was planarized prior to reactive ion etching to account for undulation of the gate over the 4:1 aspect ratio 3D channel. The high-k dielectric and metal gate were both deposited by atomic layer deposition process to ensure conformality. After gate etch and nitride spacer formation, source/drain (S/D) implantation using As and B for nMOS and pMOS, respectively, were followed by a 10 s 1070 °C spike anneal for activation. A two stage anneal for the nickel silicide process was utilized to control faceting in the S/D regions. Standard oxide based interlayer dielectric, W plug contacts, and Al–Cu metallization complete full CMOS integration.

![Graph](image)

**Fig. 1.** (Color online) \( V_g = V_d/2 \) or \( V_g = V_d \) stress comparison for (a) nMOS or (b) pMOS FinFETs demonstrating that \( V_g = V_d \) shifts \( V_I \) more.

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a)Tel.: 518-649-1019; electronic mail: chadwin.young@sematech.org
b)Also at SVTC, 2706 Montopolis Drive, Austin, Texas 78741.
c)Also at University of Florida, Gainesville.
d)Present address: Texas A&M University.
e)Also at Inha University, Korea.
HCI on (110) and (100) channel surfaces was carried out on nMOS and pMOS FinFETs of different gate lengths (90, 110, and 250 nm, as drawn). In the HCI methodology, a stress bias is applied to the gate at a value typically above the operation voltage in an effort to accelerate degradation while applying a bias to the drain at the typical values of $V_d = V_g$ or $V_d = V_g / 2$. When exposed to this type of stress, devices become susceptible to interface trap generation and hot electron injection (from impact ionization) into the gate dielectric at the drain side of the device. The stress bias condition was set such that the $V_g - V_t$ stress condition was 1.3, 1.5, or 1.7 V with interspersed source-to-drain (S/D) and reverse drain-to-source (D/S) $I_{ds}-V_g$ sense measurements to monitor the $V_t$ shift ($\Delta V_t$) and $I_{dsat}$.

III. RESULTS AND DISCUSSION

Figure 1 shows the $\Delta V_t$ time dependence for (a) nMOS and (b) pMOS stress condition dependences at $V_d = 2.0$ V for (110). The $V_t$ shifts more at $V_g = V_d$ stress condition for both nMOS and pMOS FinFETs. To analyze the reason, Figs. 2 and 3 illustrate two-dimensional (2D) device simulation re-
results for impact ionization (II) rates at the (a) $V_g = V_d/2$ or (b) $V_g = V_d$ stress condition. The magnitude of II rate is on the vertical scale, and the II rates are highest at the gate edges near source or drain [see FinFET in Fig. 2(a)] as explained below. The structural parameters used in the simulations were selected to emulate the 90 nm CMOS metal/high-$\kappa$ FinFET with the channel length ($L_C$) and equivalent oxide thickness of 90 and 1 nm, respectively. The doping concentration of the channel ($N_g$), source/drain ($N_{SD}$), and extension ($N_{ext}$) are $10^{15}$, $10^{20}$, and $5 \times 10^{19}$ cm$^{-3}$, respectively, and the doping gradient of extension ($\sigma_{ext}$) is assumed to be 2 nm/decade. We used the 2D numerical simulator, Taurus-Medici.$^5$ Under a high gate voltage condition ($V_{GS} = V_D = 2.5$ V), and thus high drive current, the body potential under the gate increases because of the Ohmic voltage drop at the source extension with floating body. Thus, the additional peak of the electric field appears at the source junction with increasing $V_{GS}$ due to the elevated body potential.$^6$ Additional impact ionization at the source, as shown in Figs. 2(b) and 3(b), induces further hot carrier degradation. This can be severe because of higher injection efficiency due to the higher voltage difference between the gate and the source. Under normal operating conditions (low gate bias), HCI at the source junction is negligible. However, high gate voltages applied to accelerate degradation can activate the additional HCI process at the source junction, which may result in erroneous lifetime prediction.$^6$

Measured results in Figs. 4 and 5 illustrate the $\Delta V_t$ for various $V_g - V_t$ conditions after 1000 s of stress. Similar trends are seen independent of orientation except for the pMOS (110) case [Fig. 4(b)]. The (110) surface is expected to have more interfacial silicon bonds for possible breakage during stress,$^3$ however, the results show no appreciable degradation over the (100) surface possibly due to the novel sidewall smoothing and passivation process.$^4$ During fabrication, the pMOS (110) devices have a more pronounced overlapped gate structure at the source/drain, and implanted B diffuses efficiently along this surface thereby effectively reducing the channel length causing enhanced HCI degradation. Therefore, this device cannot be directly compared with the others, but it is included for completeness. The insets of Figs. 7 and 8 show the channel length dependence where these results illustrate that HCI degradation increases as the fin length decreases or stress voltage increases.$^7$ In addition, the $V_g > V_d$ condition needed to enhance interface state generation did not occur since $V_g = V_d$. To confirm oxide trapped charge and/or interface state generation during stress, $I_{dsat}$ was compared between S/D $I_d$ and swapped D/S $I_d$. $I_{dsat}$ degradation has a similar trend for comparable devices on both orientations (Fig. 6). An example of swapping the source/drain re-
veals similar $I_{	ext{desat}}$ degradation demonstrating impact ionization at the source and drain (Fig. 6, inset).

Planar high-$\kappa$ devices have previously demonstrated that “cold” carrier trapping,$^{8-10}$ and possible hole accumulation in the fin body could convolute the HCI degradation when monitoring $\Delta V_t$. Therefore, introducing a cold carrier “discharge”$^{10}$ or forward biasing the source junction can de-trap cold carriers and remove channel holes, respectively, separating them from HCI degradation. The results illustrate negligible $V_t$ recovery (Fig. 7) suggesting (a) no significant cold carrier trapping (expected for 2 nm high-$\kappa$ film$^{11}$), and no significant hole accumulation (Fig. 8) in the body of the fin for 90 nm nMOS FinFETs on (110).

IV. CONCLUSION

HCI degradation on nMOS and pMOS FinFETs with HfSiON/TiN on (100) and (110) surface orientations was studied. As expected, HCI degradation increases as stress voltage increases and as fin length decreases, irrespective of substrate orientation due to impact ionization at both the source and drain sides. $V_t$ shifts show no significant differences due to substrate orientation. Negligible cold carrier trapping or hole accumulation was detected thereby demonstrating that $\Delta V_t$ was caused primarily by the trapped charge/interface state generation caused by impact ionization.


$^2$Tsung-Yang Liow et al., Tech. Dig. VLSI Symp. 2006, 56.


$^4$M. M. Hussain (unpublished).


