Effects of Film Stress Modulation Using TiN Metal Gate on Stress Engineering and Its Impact on Device Characteristics in Metal Gate/High-\(k\) Dielectric SOI FinFETs

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Abstract—In this letter, the effects of TiN-induced strain engineering on device characteristics for a metal gate/high-\(k\) silicon-on-insulator fin-shaped field-effect transistors were studied. From a convergent-beam electron-diffraction analysis and simulation study, a 3-nm TiN electrode was found to lead to significantly higher tensile stress on the Si substrate than a 20-nm TiN electrode. This high-stress-induced fast bulk carrier generation results in the transient current–time characteristics. Therefore, 3- and 20-nm TiN electrodes are the excellent choice for nMOSFETs and pMOSFETs, respectively, which is from the standpoint of strain engineering, threshold voltage \(V_{th}\), and performance. Due to the metal-induced stress, \(I_{dsat}\) improvements of 15% and 12% for nMOSFETs and pMOSFETs, respectively, were achieved.

Index Terms—High-\(k\) dielectric, metal-induced strain, silicon-on-insulator (SOI) fin-shaped field-effect transistors (FinFETs).

I. INTRODUCTION

T O FURTHER improve the device performance within given physical geometry limits, various strain techniques, such as strained silicon-on-insulator (SSOI), silicon–germanium (SiGe) substrate, dual stress liner (DSL), and stress memorization, are being intensively investigated as ways to enhance device performance [1]–[5]. A thin metal gate electrode was reported to be used for a process-induced stressor layer [6], [7]. It is known that a thin metal layer intrinsically induces a certain amount of stress depending on the deposition method, film thickness, and thermal treatment [8]. By selecting the right materials, it may be possible to use dual metal gate electrodes to apply stresses on the channel. Previous studies have demonstrated metal-induced strain and mobility improvements [6], [7].

Silicon-on-insulator (SOI) fin-shaped field-effect transistors (FinFETs) are some of the promising solutions for future high-performance and low-power CMOS applications because of their excellent scalability and process compatibility [9]–[11]. Due to their inherent lower channel doping, effective work-functions in the range of 250–500 meV are preferred for SOI FinFETs [12], which can provide more latitude in selecting a metal gate electrode. Unlike a planar device, the effects of metal-induced strain in FinFETs can be different because the metal layer encapsulates the Si fin and can more effectively apply stress. However, some reports have addressed an approach to metal-based strain engineering in SOI FinFETs. In this letter, we report the effects of metal-induced strain engineering on FinFET device characteristics, such as transconductance and saturation current, in conjunction with physical and numerical analysis methods. Bulk carrier-generation characteristics were also measured as an indirect way of determining Si fin stress.

II. EXPERIMENTAL

Samples for this letter were prepared by a sub-60-nm CMOS metal/high-\(k\) FinFET process with different TiN thicknesses on a (100) SOI wafer. After the Si fin etching with a nitride hard mask, a \(H_2\) anneal was carried out, reducing surface roughness. Three nanometers of HiO\(_2\) was deposited by atomic layer deposition (ALD). For the gate electrode, 3–20-nm ALD TiN was deposited, which is followed by an amorphous Si film. To control the short-channel effects, the regions with and without a lightly doped drain were formed in nMOSFETs and pMOSFETs, respectively. After the nitride spacer formation, source–drain implantation and a NiSi process were performed. The inversion oxide thickness \((t_{inv})\) ranged from 1.3 to 1.4 nm, and the width and height of the fin were about 30 and 70 nm, respectively, as shown in Fig. 1(a). A typical channel length in this letter was 60 nm. The transistor drain current–gate voltage \((I_d-V_g)\) characteristics are shown in Fig. 1(b). For both devices, the drain-induced barrier leakage (DIBL) was less than 100 mV, and the subthreshold slope was about 85 mV/dec at the 60-nm channel length.
III. RESULTS AND DISCUSSIONS

To quantify the strain at the silicon channel, a convergent-beam electron-diffraction (CBED) analysis was carried out on the 3- and 20-nm ALD TiN on 3-nm HfO₂ dielectric planar MOS capacitor structures [Fig. 2(a)] [16]. For the 3-nm TiN sample, the metal-induced Si lattice displacements at 50 nm below the Si surface were 0.44% for the horizontal direction (\( \sigma_{yy} \)). These lattice mismatches decreased in the 20-nm TiN samples, which were 0.13% for the \( \sigma_{yy} \). The measured lattice strain showed that the 3-nm TiN film induced a higher tensile stress on Si than the 20-nm TiN film horizontally. Lim et al. [17] reported that the physical-vapor-deposition TiN film stress increased with decreasing thickness due to the change of the preferred orientation. To further reduce the TiN below 3 nm, a TiN island structure is formed rather than a layer, and the TiN-induced strain cannot be measured by the wafer bowing test. The calculated stress difference was 390 MPa for \( \sigma_{yy} \). However, these measurements have been done on planar substrates, and the stress in the fin can be different.

Two-dimensional numerical simulation was performed to check the actual metal-induced stress in the Si-fin [13]. For the stress simulation, a Young’s modulus for the TiN metal was 550 GPa, which is as taken from the literature [14], [15]. The metal film stress value was measured from the wafer bowing test. Fig. 2(b) shows the contour plots of the projected stress from the TiN layer into the Si fin. Considering that the 3-nm TiN induced higher compressive stress, the stress in the Si fin was tensile. The 3-nm-TiN-induced tensile stress in Si was higher than that of the 20-nm TiN sample. For both cases, the top corner of the fin exhibited the highest projected strain. However, the bottom corner of the fin stressed compressively, which is attributed to the recess of the buried oxide. The simulation results exhibited similar behavior, with the CBED results showing that the thicker TiN resulted in a lower tensile strain on the Si substrate.

We looked at how this metal-induced strain affects the device performance. Fig. 3 shows the normalized transconductance for the 3- and 20-nm TiN samples, which is directly proportional to the carrier mobility, which is shown as

\[
\frac{G_m L_g}{C_{ox}} = W \mu V_{ds}.
\]

As clearly shown, the electron mobility for the 3-nm TiN devices was higher than that of the 20-nm TiN samples, and
the 20-nm TiN showed higher hole mobility. These results are further evidence that a thin metal electrode can induce more strain. In addition, in our metal-induced strain FinFET devices, the transverse stress in the channel direction is still valid for enhancing the device performance. Generally, strain leads to a bandgap narrowing, which increases the junction leakage for enhancing the device performance. For the 3-nm TiN devices recovered more quickly than the 20-nm TiN.

In summary, we demonstrated TiN-induced strain engineering for a metal gate/high-κ SOI FinFET. The physical analysis, simulation, and carrier-generation characteristics showed that the 3-nm TiN induced higher channel stress than the 20-nm samples. For the nMOSFET, a thinner TiN was found to improve the tensile stress on the Si substrate. Due to the metal-induced strain, the 3-nm TiN induced higher channel stress than the 20-nm samples. For the nMOSFETs and pMOSFETs, respectively, were achieved.

Therefore, the metal-induced strain engineering can be exploited for enhanced performance; however, further study is required for its implementation in a CMOS process flow.

IV. CONCLUSION

In summary, we demonstrated TiN-induced strain engineering for a metal gate/high-κ SOI FinFET. The physical analysis, simulation, and carrier-generation characteristics showed that the 3-nm TiN induced higher channel stress than the 20-nm samples. For the nMOSFETs and pMOSFETs, respectively, were achieved.

Therefore, the metal-induced strain engineering can be exploited for enhanced performance; however, further study is required for its implementation in a CMOS process flow.

REFERENCES


[13] TSUPREM is a Trademark of Synopsys.


