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The effect of interfacial layer properties on the performance of Hf-based gate stack devices

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The influence of Hf-based dielectrics on the underlying SiO2 interfacial layer (IL) in high-k gate stacks is investigated. An increase in the IL dielectric constant, which correlates to an increase of the positive fixed charge density in the IL, is found to depend on the starting, pre-high-k deposition thickness of the IL. Electron energy-loss spectroscopy and electron spin resonance spectra exhibit signatures of the high-k-induced oxygen deficiency in the IL consistent with the electrical data. It is concluded that high temperature processing generates oxygen vacancies in the IL responsible for the observed trend in transistor performance. © 2006 American Institute of Physics.

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I. INTRODUCTION

To sustain the historical rate of transistor scaling, the conventional SiO2 gate dielectric layer must be replaced with a material that offers a higher dielectric constant k. HF oxide and Hf silicate thin films, with and without some form of nitrogen, currently being considered for gate dielectric applications result in a multilayer structure that includes an SiO2-like layer either spontaneously or intentionally formed at the interface with the substrate.1 Several groups have shown that the k value of this interfacial layer (IL) may be significantly greater than that of bulk stoichiometric SiO2.2-5 Although it has been proposed that the increase in the dielectric constant is a direct result of HF diffusion into the IL to form Hf silicate,2,4 an alternative explanation based on observed transistor electrical characteristics and supported by high resolution chemical and spectroscopic analysis strongly indicates that the high-k film modifies the stoichiometry of the underlying SiO2 layer by rendering it oxygen deficient.3,6 These observations are consistent with ab initio modeling of the SiO2/Si stack that calculates the contribution of underoxidized Si atoms to an increase in the SiO2 dielectric constant.7 O deficiency may also be expected to induce a higher density of fixed charges in the IL associated with the Si–Si defects. Since this interfacial layer plays a critical role in the performance of advanced complementary metal-oxide silicon (CMOS) field effect transistor (FET) devices, it is important to understand the mechanism of its modification. However, quantitative analysis of the change in the IL k value requires an accurate determination of the physical thickness, which is complicated by the need to distinguish chemical intermixing from microroughness at the interface with high-k films.8 To address the high-k/SiO2 interaction systematically and decrease the uncertainty with regard to IL thickness, a set of transistor gate stacks has been fabricated by depositing Hf-based films on well-defined thermal SiO2 layers of different thicknesses. This sample set has been characterized using a combination of electrical and physical analytical techniques.

II. ELECTRICAL MEASUREMENTS

A. IL in a Hf silicate stack: Permittivity

Hf silicate films, herein referred to as HfSiOx, of incremental thicknesses have been produced on various starting surfaces by atomic layer deposition (ALD), described in detail previously,9 and fabricated as gate dielectric transistors [Hf(O)2]0.8(SiO2)0.2/TiN] using a standard CMOS process that includes a 1000 °C/5 s dopant activation annealing. The starting surfaces, before Hf silicate deposition, were prepared by either using an HF-last treatment of the Si substrate, which resulted in less than 3 Å of chemical SiO2, or growing thermal 21 Å SiO2 layers that are then scaled down to 6, 11, and 19 Å by a calibrated wet etch back process.10

In the equivalent oxide thickness (EOT) versus high-k physical thickness plots of Fig. 1 [EOT = (k_h/k_m)th], where k_h and k_m are the dielectric constants of the high-k film and SiO2, respectively, and th is the high-k film physical thickness] all trend lines are parallel because their slopes are defined by the permittivity (k value) of identically processed high-k films. Since the total EOT of each gate stack measured in Fig. 1 is known, one can estimate the EOT of each IL as the difference between the measured value and the

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EOT of the high-$k$ film. The latter value is extracted based on the $k$ value of the high-$k$ film (derived from the slope of the EOT versus physical thickness dependence in Fig. 1) and its physical thickness. The obtained EOT values of the ILs were verified to be the same for each set of gate stacks with a given high-$k$ thickness in Fig. 1. Based on the postprocessing physical thickness measurements, the extracted EOT values of the ILs may then be used to estimate their corresponding $k$ values. As illustrated in the high resolution transmission electron microscopy (HRTEM) cross-section images of Fig. 2, all of the fully processed ILs were found to be $\sim$11 Å thick, except for the 19 Å starting IL, which appeared unaffected. Although this comparative analysis is quite significant, HRTEM determination of the IL thickness is considered approximate since it tends to underestimate the dimension of amorphous low $Z$ (atomic weight) layers juxtaposed to crystalline films due to any interfacial microroughness. The processed IL dielectric constant (and IL relative charge discussed in the following section) versus IL starting thickness is shown in Fig. 3, which illustrates the phenomenon of a higher-$k$ value corresponding to thinner starting IL. The extracted $k$ value of each IL is significantly higher than the calculated effective dielectric constant for the same thickness of SiO$_2$, as shown in the inset in Fig. 3. In particular, the resultant permittivity of the 11 Å IL with a starting thickness of 11 Å is $\sim$6, while calculations predict the $k$ value for the 11 Å SiO$_2$ film at <5, indicating that the ILs have been modified by high-$k$ processing. The major contribution to the higher-$k$ value (above the bulk value of 3.9) of a thin SiO$_2$ film is shown to come from the underoxidized Si atoms, in particular, Si$^{2+}$, in the substoichiometric transitional layer near the SiO$_2$/Si interface. This suggests that the observed boost in the $k$ value of the SiO$_2$ layer in the high-$k$ gate stack may result from a higher degree of its oxygen deficiency.

### B. IL in a Hf silicate stack: Charge density

The flatband voltage ($V_{fb}$) versus EOT relationship of each film system discussed previously is plotted in Fig. 4. This dependence is described by the following equation:

$$V_{fb} = \Phi_{ms} - \frac{Q_i}{k_{ox}} - \frac{\rho_0(k_h/k_{ox})EOT^2}{2k_{ox}} - \frac{Q_f}{k_{ox}}. \quad (1)$$

where $\Phi_{ms}$ is the gate electrode work function value, $Q_i$ is the fixed charge at the high-$k$/IL interface, EOT$_h$ and EOT are the EOT values of the high-$k$ layer and the total given gate stack, respectively, $\rho_0$ is the volume density of fixed charges in the high-$k$ film, and $Q_f$ is the effective fixed charge density at the IL/Si substrate interface ($Q_f$ represents a projection of the total charge in IL to the IL/Si interface). Using IL EOT values obtained from the data in Fig. 1 and the parameter values estimated from the extended set of experiments on the terraced oxide test structure, the work func-

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**FIG. 1.** Dependence of EOT vs high-$k$ physical thickness for different thicknesses of starting SiO$_2$ interfacial layers (IL).

**FIG. 2.** HRTEM images of fully processed 3 nm ALD HfO$_2$ transistor gate stacks built with <3 Å (HF-last predeposition clean) and 11 Å starting SiO$_2$ ILs.

**FIG. 3.** Postprocessed IL dielectric constant and fixed interface charge (relative to the reference sample of the thickest interfacial layer) vs thickness of starting IL.

**FIG. 4.** Flatband voltage vs EOT dependence for different starting ILs. The fit (lines) is obtained by using experimentally estimated values of the work function $\Phi_{ms}$, high-$k$ bulk, $\rho_0$, and high-$k$/IL, $Q_f$, charge densities, with the only fitting parameter being a value of IL charge $Q_f$. 

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tion value for the TiN/HfSiO stack of 0.5 eV, high-k bulk charge density of $0.5 \times 10^{17}$ cm$^{-3}$, and constant value of the fixed charge at the high-k/IL interface of $1 \times 10^{12}$ cm$^{-2}$—the data in Fig. 4 were fit with Eq. (1) by varying a single parameter; the effective fixed charge at the gate stack/substrate interface ($Q_f$). The $Q_f$ values (with respect to the reference $Q_f$ value in the thickest IL) versus the IL starting thickness are plotted in Fig. 3. DCIV measurements (not shown) verified the trend of the interface charge changes among the stacks with different starting ILs.

In summary, results in Fig. 3 suggest that high-k processing has a stronger influence on thinner starting (preprocessing) SiO$_2$ IL, in that the final (post-high-k processing) IL demonstrates a higher-k value accompanied by higher interface fixed charges.

This trend in fixed interface charges has been correlated to carrier channel mobility (extracted by the NCSU MOB2D program). Since the mobility values obtained using dc transistor drain current data may be affected by the fast (microseconds) transient charging (FTC) at the preexisting electron traps in the high-k film, the applied a fast pulsed drain current-gate voltage ($I_dV_g$) technique described previously, which has been shown to exclude the FTC effect in the drain current and, consequently, in the mobility measurement. The mobility results for two sets of gate stacks comprised of different high-k film thicknesses are plotted versus fixed interface charges in Fig. 5. The decrease in mobility is clearly correlated with an increase in the fixed charges density and higher-k values of the ILs, as in Fig. 3. Interestingly, the physical thicknesses of the ILs in all these devices are approximately the same (with the obvious exception of the thick 19 Å IL sample).

C. IL in a HfO$_2$ stack

HfO$_2$ films exhibit effects on IL similar to HfSiO, albeit more profound: thinner starting interfaces are affected to a greater degree (greater k change) by the overlying HfO$_2$ film, which correlates to lower channel carrier mobility (Fig. 6). Since the interface state density ($N_{it}$) shows only a slight increase for thinner starting SiO$_2$ layers (Fig. 7) $N_{it}$ is not sufficient to cause the observed mobility differences among different IL samples, indicating the high-k process-induced generation of fixed charges in the SiO$_2$ interface is one of the major contributors to mobility degradation.

Further insight into the effects of the overlying high-k film on electrical properties of the IL can be gained by applying a frequency-dependent charge pumping (CP) technique to the high-k transistors. This can provide information on the charge trap density profile through the dielectric thickness. CP measurements in the frequency range of 1 MHz–2 kHz were performed on devices with gate stacks made up of 3 nm ALD HfO$_2$ film deposited on either 1.1 or 1.4 nm of thermal SiO$_2$ layers (followed by a TiN gate electrode). The CP measurements were repeated after the applying electrical stress (3 V for 300 s). Since measurement frequencies at the given CP test condition define the depth (counting from the substrate) of accessible charge traps, one can convert frequency dependence of the trap density $N_{it}$ to its dependence on the distance from the IL (Fig. 8). $N_{it}$ in both ILs increases closer to the HfO$_2$ film while $N_{it}$ values at the same distance from the high-k film are similar in both gate stacks before and after the stress. Additionally, $N_{it}$ values tend to quickly saturate with stress time. These results indicate that the interaction of the IL with the overlying high-k HfO$_2$ film may generate charge traps and precursor defects ("weak" spots such as Si–Si defects), which could be converted to traps by subsequent electrical stress.

Overall, electrical data point to an appreciable modification of the composition of the interfacial SiO$_2$ layer caused by high-k processing.
III. PHYSICAL CHARACTERIZATION

A. Hf in IL

To understand the physical origin of high-k-induced defects in the IL, HfO2/SiO2 film systems were characterized using spherical aberration corrected scanning tunneling electron microscopy (STEM), which has a resolution sufficient to image individual Hf atoms in SiO2 with ~5 Å depth precision. Samples representative of the above electrically characterized gate stacks were systematically prepared to reproduce and isolate conditions corresponding to critical transistor fabrication process steps. This was accomplished by imaging the IL following high-k deposition and comparing the results with otherwise identical film systems following a high temperature annealing at 1000 °C/10 s. STEM images of fully processed 3 nm thick ALD HfO2 deposited on thermally grown 2 nm thick SiO2 are shown in Fig. 9. The highlighted bright spots in Fig. 9 result from detection of local high density Z-contrast sensitivity corresponding to individual Hf atoms that have diffused into the IL during the annealing process (no Hf atoms were detected in IL in the as-deposited sample). This overall low Hf density, in the range of \( \leq 1 \times 10^{13} \) cm\(^{-2}\), excludes the possibility of Hf silicate formation in the IL. This finding is consistent with thermodynamic phase diagrams that indicate an 80 mol. % HfO2 silicate phase separates to form crystalline HfO2 and amorphous SiO2 during a 1000 °C/10 s annealing. (It is also interesting to note a very small diffusion coefficient \( D \) for the Hf atoms in SiO2, \( D = 2.5 \times 10^{-18} \) cm\(^2\)/s at 1000 °C, which would severely restrict the Hf diffusion.) While x-ray photoelectron spectroscopy (XPS) has been widely used to evaluate the chemical characteristics of the buried IL of annealed HfO2/SiO2 film systems, spectra interpretation has been inconsistent since both Hf silicate and oxygen-deficient SiO2 produce a shift of the Si\(^{4+} \) 2p peak towards lower binding energy. However, since the Hf 4f core level spectra, obtained by variable incident photon energy depth profiling through the HfO2 film and IL, do not exhibit a corresponding shift to a higher binding energy, the Si\(^{4+} \) 2p peak shift, which increases closer to the probed IL volume to the high-k film, can be attributed to O deficiency. Furthermore, since no Hf density gradient across the IL is detected (Fig. 9), Hf in the IL is most likely the result of a limited quantity of initially weak-bonded and loose atoms (so-called renegade Hf atoms).

B. O deficiency of IL

The phenomenon of oxygen removal from the underlying SiO2 layer due to high-k film deposition/processing is captured in the electron spin resonance (ESR) spectra of Fig. 10. The dominant electrically active defects at the Si/SiO2 interface are \( P_b \) centers (\( P_{b0} \) and \( P_{b1} \)), which consist of the dangling bonds of the Si substrate atoms (an unpaired electron on a Si atom back bonded to three other Si atoms of the substrate) at the Si/SiO2 interface. The most significant signature of defects in the bulk SiO2 observed here is consistent with \( E' \) center defects, which involve an unpaired electron residing on a Si atom back bonded to three oxygen. These ESR signatures usually correspond to oxygen vacancies but can also result from single oxygen deficient silicon. The data

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**FIG. 8.** Trap density vs distance from the Si substrate before and after the stress. Illustration on the right schematically shows two studied gate stacks where a high-k-induced trap density profile is presented as a contrast gradient of the shaded area.

**FIG. 9.** STEM images of the 3 nm HfO2/2 nm SiO2 stack after 1000 °C annealing. Stray Hf atoms in the IL are circled.

**FIG. 10.** ESR spectra collected in the stacks containing a 2 nm thermal SiO2 layer with 3 and 30 nm ALD HfO2 film deposited on top.
in Fig. 10 show the density of \( P_{p0} \), \( P_{p1} \), and \( E' \) centers associated with low temperature deposition (300 °C) of HfO\(_2\) on 2.0 nm thermal SiO\(_2\) followed by a 700 °C/60 s post deposition annealing in N\(_2\) ambient. While the density of \( P_{p0} \) and \( E' \) states in IL is greater in the 3 nm HfO\(_2\) sample than the sample without HfO\(_2\) (not shown), the thicker, 30 nm HfO\(_2\) film, produced by the identical process, clearly generated more O vacancies at the SiO\(_2\)/Si interface and in the bulk IL. The density of \( P_{p0} \) centers is routinely maintained at an acceptable level through hydrogen passivation during forming gas annealing, although the defect density remains slightly higher for thinner starting interfaces, as discussed previously and illustrated in Fig. 7. A potential consequence is that hydrogen could be released during device operation, under elevated temperature or under certain gate voltage conditions, thereby affecting device reliability.

An additional investigation of the compositional change of the 2 nm SiO\(_2\) IL in the HfO\(_2\) gate stack caused by the high temperature annealing (1000 °C/10 s) was conducted using high angle annular dark field scanning transmission electron microscopy (HAADF-STEM) in combination with electron energy loss spectroscopy (EELS) (measurement details are described in Ref. 17). These measurements produce atomic-number sensitive “Z-contrast” images and acquire the Si \( L_{2,3} \) edge profile, respectively, to obtain the Si chemical intensity profile gradient as a function of position across the interfacial region of the HfO\(_2\)/SiO\(_2\)/Si film system. The Si \( L_{2,3} \) edge signal collected in the bulk of the SiO\(_2\) IL (the probe size was 1.5 Å), illustrated in Fig. 11, exhibits a low energy “shoulder” (indicated by an arrow) in the postannealed sample, which corresponds to Si atoms in various coordination states (rather than just Si\(^{4+}\) of the stoichiometric SiO\(_2\), as seen in the spectrum collected at the same cross-section position in the IL of the as-deposited sample) indicative of a higher density of oxygen vacancies.

![Graph](image)

**FIG. 11.** ADF TEM image and Si \( L_{2,3} \) edge EELS taken at the identified positions (colors) in the 3 nm HfO\(_2\)/2 nm SiO\(_2\) stack before (a) and after (b) annealing. The increase in signal from undercoordinated Si atoms in SiO\(_2\) after annealing is shown by an arrow bar.

### C. Coarse O deficiency of IL

Since O vacancy formation in SiO\(_2\) is thermodynamically preferable to HfO\(_2\),\(^{22}\) while metal oxides (similar to perovskites), in general, are rich in oxygen vacancies,\(^{23}\) these factors may constitute a driving force for the oxygen drift from IL to the metal oxide dielectric, which probably occurs more efficiently during the metal oxide crystallization phase. This mechanism suggests that a higher density of oxygen vacancies in the high-\( k \) film should generate greater oxygen deficiency in the SiO\(_2\) IL. To verify this prediction, highly oxygen-deficient HfO\(_2\) film of about 3 nm was deposited on a 1.1 nm chemical SiO\(_2\) layer (grown by an O\(_3\) treatment of the Si substrate) followed by a 1000 °C/10 s annealing. Oxygen deficiency in HfO\(_2\) was achieved by reducing either the duration of the O\(_3\) pulse from 1.5 to 0.1 s during the ALD cycles or the O\(_3\) flow from 150 to 50 g/m\(^3\). The ESR spectra collected on these samples show significantly higher oxygen deficiency of IL than the samples prepared with the standard HfO\(_2\) ALD process, as shown in Fig. 12 (for the sample with the shortened O\(_3\) cycle). The spectra demonstrate the generation of two \( E' \) variants, \( E'_g \) (zero crossing \( g = 2.0005 \)) and another variant, quite possibly very similar to the \( E'_s \) (zero crossing \( g = 2.0020 \)), which represents oxygen-deficient silicon back bonded to oxygen. The intensity of the \( E' \) signal implies that the density of the oxygen-deficient silicons is about \( \approx 1 \times 10^{19} \) cm\(^{-3}\). ESR data likely underestimate the actual density of the oxygen vacancies since only the paramagnetic oxygen defects contribute to these measurements.

Detailed changes in the ESR spectra of the IL caused by the deposition and processing of the standard HfO\(_2\) film are shown in Fig. 13. \( P_{p0} \) and \( E' \) centers initially present in the IL oxide were passivated during the high-\( k \) deposition due to the O\(_3\) oxidation cycle employed in this ALD process.\(^{9}\) A subse-
Although an IL increases the total EOT of the gate dielectrics, the IL is a critical component of the gate stack contributing to higher channel carrier mobility by reducing carrier scattering by soft optical phonons, fixed charges, random grain orientation, etc., in the high-$k$ films. Our results indicate that further improvement of high-$k$ device performance requires better control over the stoichiometry of the interfacial SiO$_2$ layer achievable, in particular, by using a higher quality starting SiO$_2$ layer and optimizing the high-$k$ deposition process.

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