Effects of interfacial layer growth on the electrical characteristics of thin titanium oxide films on silicon

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(Received 22 September 1998; accepted for publication 30 March 1999)

Effects of interfacial layer growth on reactively sputter-deposited TiO₂ films were studied. Leakage current was reduced to $10^{-8}$ A/cm² at $+1$ V after annealing in oxygen ambient and showed tunneling-like temperature dependence. As the interfacial layer grew, interface states and hysteresis were improved significantly. However, the reliability was degraded as the annealing temperature increased. © 1999 American Institute of Physics. [S0003-6951(99)03121-6]

Binary metal oxides such as CeO₂, Y₂O₃, Al₂O₃, Ta₂O₅, and TiO₂ (Refs. 5 and 6) have been studied as alternative gate dielectrics for scaled metal–oxide–semiconductor field-effect transistors to overcome the scaling limit of conventional gate oxides. Among them, TiO₂ has received a lot of attention recently because of its high dielectric constant. However, the dielectric properties of TiO₂ are known to be degraded by several interfacial reactions with silicon, such as retarded crystallization, intermixing with SiO₂, and growth of a low dielectric constant interfacial layer. Thus, the reported dielectric constants of TiO₂ films are scattered in the range of 16–52, 4–40, and 20–86, 11 while that of rutile bulk TiO₂ is 170 along the optic axis and 89 perpendicular to the optic axis. These adverse effects will become worse at the thin-film regime (<10 nm), where the effects of interfacial reactions are more substantial. However, only a few works have been done to assess the effects of the interfacial layer and the reliability characteristics of TiO₂ have not been studied yet. In this letter, we present the effects of the interfacial layer on the electrical characteristics of 10 nm TiO₂ films with a comparison of TiO₂ films deposited on a metal substrate.

TiO₂ films were reactively sputter deposited on a bare silicon wafer and an iridium-coated wafer, respectively, at a pressure of 10 mTorr of Ar with 20% O₂ using dc magnetron sputtering. A platinum electrode (thickness ~100 nm) was used. After wet etching the electrode, the samples were annealed at various temperature ranging from 500 to 900 °C in N₂ or O₂ for 5 min. The film thickness and refractive index were measured using a single-wavelength ellipsometer with a single-layer model and examined with scanning electron microscopy. The crystalline phase of the annealed film was analyzed by x-ray diffraction.

The equivalent oxide thickness (EOT) extracted from the accumulation capacitance stayed fairly constant after annealing while the physical thickness measured with the ellipsometer increased (Fig. 1). The unpublished x-ray diffraction analysis data showed that the peak from the anatase phase in as-deposited TiO₂ grew as the O₂ annealing temperature increased. The refractive index of the TiO₂ films increased from 2.3 to 2.5 after the 700 °C annealing, but decreased to 2.25 again after the 800 °C annealing. The decrease of the refractive index indicates that the interfacial layer growth becomes dominant beyond this temperature. The slow increase of the EOT is a result of a trade-off between the crystallization and interfacial layer growth.

The leakage current of the O₂ annealed capacitors decreased rapidly to $10^{-7}–10^{-8}$ A/cm² after annealing while that of the N₂ annealed capacitors fluctuated around the $10^{-3}–10^{-4}$ Al/cm² range (Fig. 1). The decrease in leakage current by the O₂ anneal seems to be related to the growth of interfacial layer and the reduction of oxygen vacancies. The leakage current of the metal–insulator–silicon (MIS, Pt/TiO₂/Si) capacitor showed a tunneling-like temperature dependence while that of the metal–insulator–metal (MIM, Pt/TiO₂/Ir) capacitors showed the strong temperature dependence ($E_a=0.78$ eV for both bias polarity) (Fig. 2). This trend indicates that the tunneling current passing through the interfacial layer limits the total leakage current of the MIS capacitor.

By comparing the EOT of the MIS and MIM capacitors, the thickness of the interfacial layer was found to be about 2.2 nm (Fig. 3). This value is very close to our previous transmission electron microscopy observation. The nearly constant thickness of the interfacial layer at different physical thickness indicates that the interfacial layer was grown at the initial step of the deposition process. From the reciprocal slope of Fig. 3, the dielectric constant of TiO₂ deposited on metal was calculated to be about 95. The similar slope of the

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FIG. 1. The equivalent oxide thickness and the gate leakage current at $+1$ V changed by the postdeposition annealing.

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MIS and MIM capacitors indicates that the dielectric constant of the TiO$_2$ layer deposited on top of the interfacial layer is close to that of the TiO$_2$ deposited on metal. Since the additional growth of the EOT by annealing was also thickness independent, the growth of the interfacial layer seems to be due to the reaction-limited oxidation.

Although the leakage current decreased as the thickness of the interfacial layer grew, the time zero dielectric breakdown voltage of the MIS capacitors degraded after annealing and the same trend was observed at the MIM capacitors. This trend implies that the breakdown of the MIS capacitor is related to the properties of the TiO$_2$ layer rather than that of the interfacial layer.

To understand this result in detail, the breakdown voltage of the MIS capacitor was measured at different TiO$_2$ thicknesses. The electric field applied to the TiO$_2$ layer and the interfacial layer were estimated, respectively, using a series capacitor model. The interfacial layer was assumed to be 2 nm of SiO$_2$ to simplify the calculation. The calculated breakdown field of the TiO$_2$ layer was nearly constant at different thicknesses while that of interfacial layer increased to an unreasonably high value. The constant breakdown field at TiO$_2$ indicates that the breakdown process is driven by the same mechanism. This result further supports our contention that the breakdown mechanism is related to the characteristics of the TiO$_2$ layer itself.

Unfortunately, although the series capacitor model showed a qualitative trend matching with the experiment, it is not an exact model because the calculated electric field at the interfacial layer is not reasonable. If the electric field is so high, the interfacial layer should breakdown first. This discrepancy may be resolved by the charge accumulation model suggested by Nishioka, Shinriki, and Mukai. According to this model, charge carriers are accumulated at the interface of the TiO$_2$ layer and the interfacial layer due to the different leakage current density and the accumulated charge limits the electric field applied to the interfacial layer below the critical breakdown field. Thus, the electric field applied to the TiO$_2$ layer increases further and the reliability characteristics are to be determined by the properties of the TiO$_2$ layer. The reasons for the reliability degradation of TiO$_2$ are not understood yet. It may be the intrinsic characteristics of crystallized TiO$_2$ or it may be caused by the degradation of the TiO$_2$ stoichiometry and silicon interdiffusion.

As for the interface properties, a substantial amount of flatband voltage shift and hysteresis were observed at the
as-deposited films. However, as the annealing temperature increased, the flatband voltage was saturated at about 0.9 V in O₂ ambient (Fig. 6). Also, the counterclockwise hysteresis of C–V curve due to the charge trapping at the negative gate bias was reduced to a negligible level. The interface state density of the TiO₂ films determined by the Terman method was comparable to thermal oxide (\(\times 10^{11}/\text{cm}^2\text{eV}^{-1}\)) after annealing.

In summary, it was found that the properties of the interfacial layer have crucial effects on the electrical characteristics of the MIS capacitor, such as leakage current, interface states, and hysteresis. However, the reliability of the TiO₂ capacitor was more affected by the properties of the TiO₂ layer itself.

This work was partially supported by SRC.